

IALAA

Minnesota 10A/10AG

LA3631P REV 1A Schematic

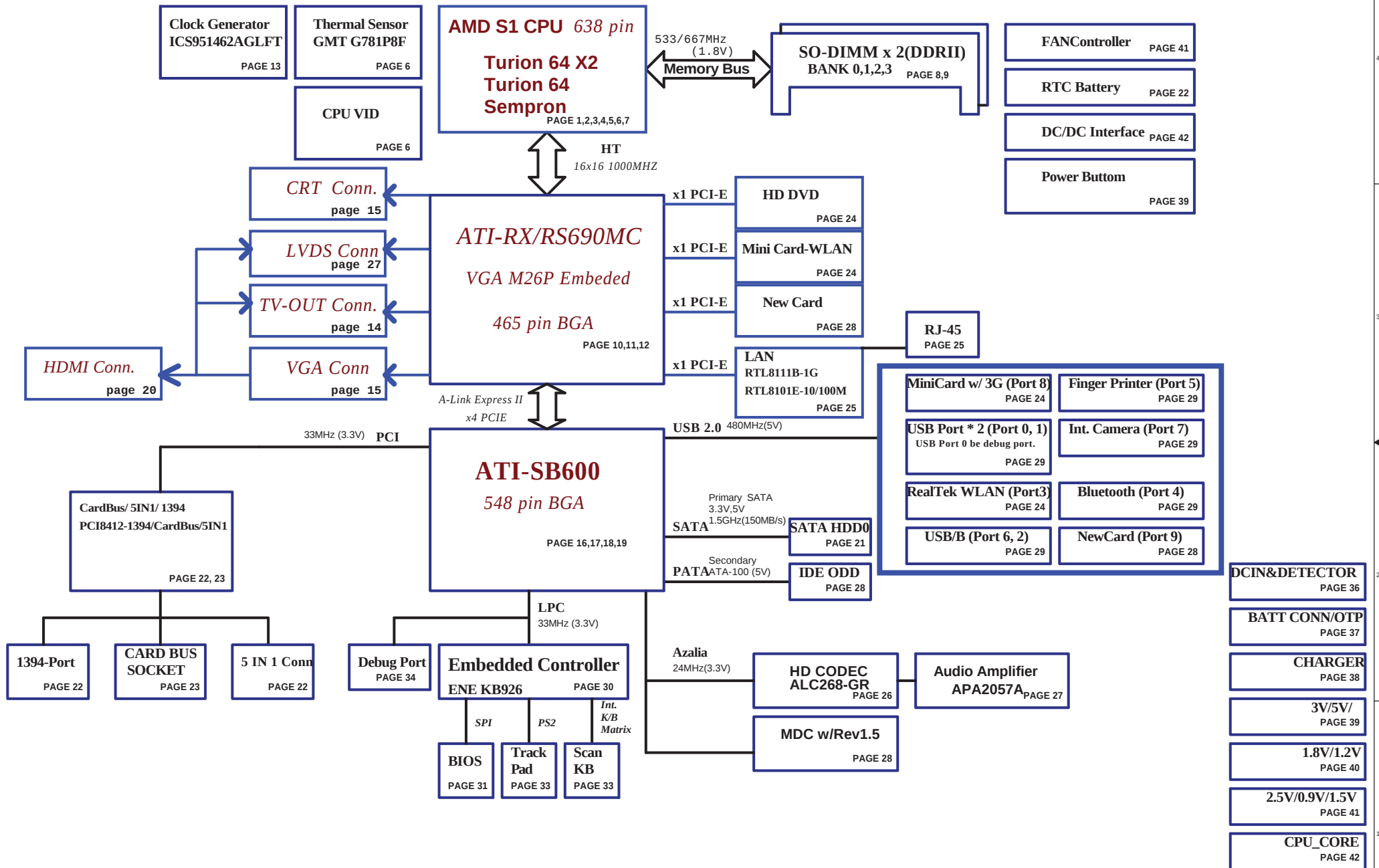
AMD Turion, Sempron/ATI RX690/RS690MC / ATI SB600
2007-05-04 Rev. 1A

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Issued Date	2007/5/4	Deciphered Date	2008/5/4	Title Cover	
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Compal confidential IALAA Minnesota10A FUNCTION BLOCK DIAGRAM

File Name : IALAA Minnesota10A LA3631P

P/N :



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+RTCVCC	RTC power	ON	ON	ON
+VSB	B+ switched power rail	ON	ON	ON
+5VALW	5V always on power rail	ON	ON	ON
+3VALW	3.3V always on power rail	ON	ON	ON
+1.2VALW	1.2V always on power rail	ON	ON	ON
+1.8V	1.8V power rail	ON	ON	OFF
+0.9V	0.9V switched power rail	ON	ON	OFF
+5VS	5VS switched power rail	ON	OFF	OFF
+3VS	3.3VS switched power rail	ON	OFF	OFF
+2.5VS	2.5VS switched power rail	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF
+1.5VS	1.5VS switched power rail	ON	OFF	OFF
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.2V_HT	1.2VS switched power rail	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#GNT#	Interrupts
1394/ CardBus/ 5IN1	AD20	2/ 2	PIRQE/F/G

EC SM Bus1 address

Device	HEX	Address
Smart Battery	16H	0001 011X b
24C16	A0H	1010 000X b

EC SM Bus2 address

Device	HEX	Address
CPU Thermal-G781P8F	98H	1001 100X b
VGA Thermal-		

ATi SB600 SM Bus address

SM Bus0 address

Device	HEX	Address
Clock GEN. (ICS951462AGLFT)		
DDR DIMM0	A4	
DDR DIMM1	A6	
Mini Card-WLAN		
Mini Card-3G		
New Card		

SM Bus1 address

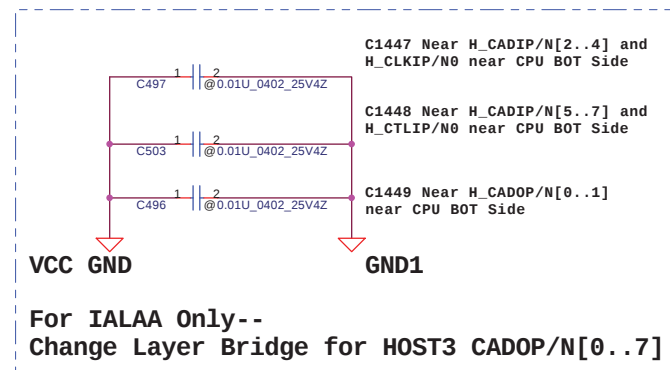
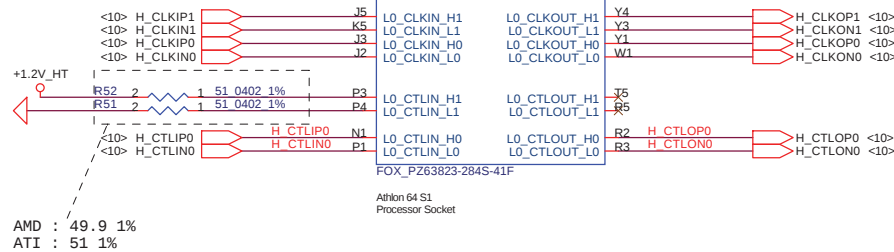
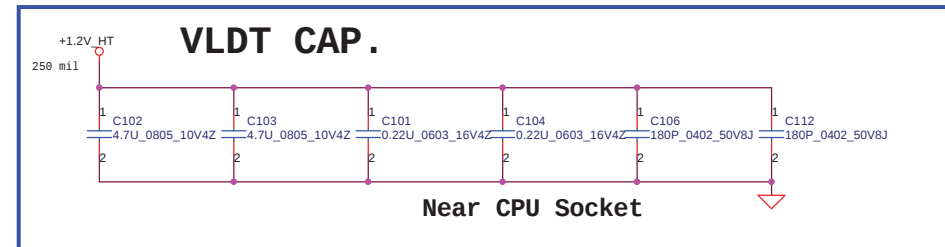
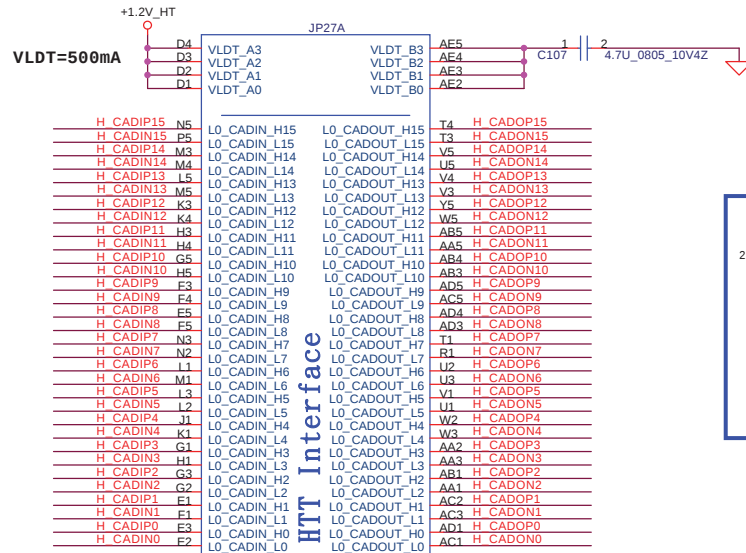
STATE \ SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	ON	OFF	OFF	OFF

ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BTN_ID	
0	
1	
2	
3	
4	
5	
6	
7	

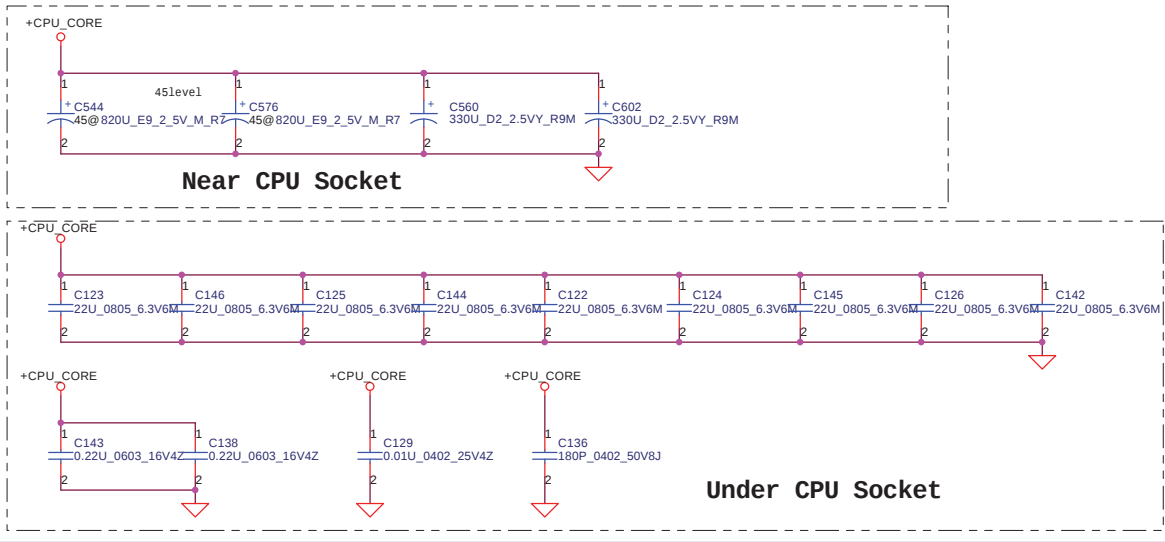
BTO	BOM STURCTURE



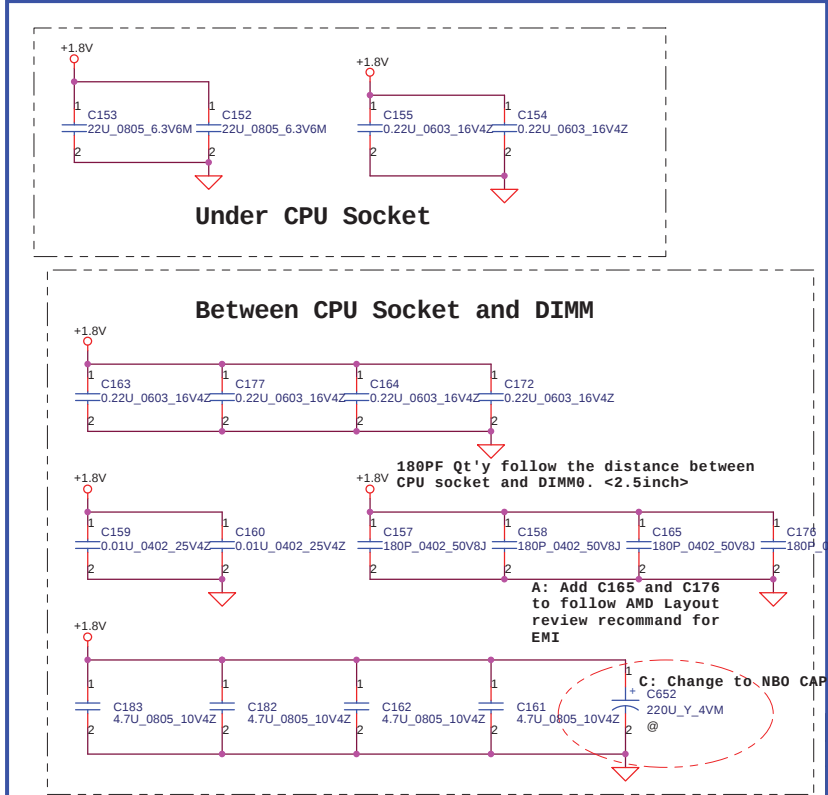


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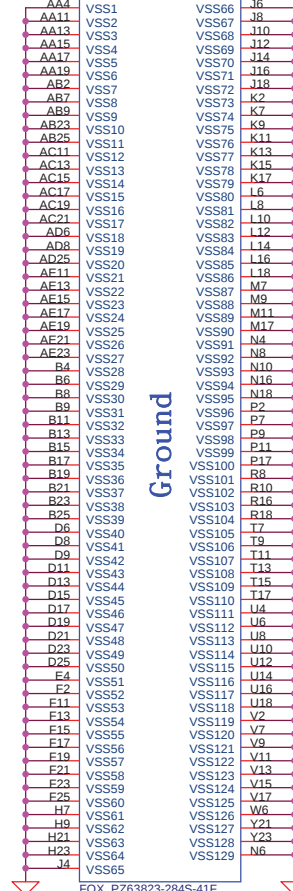
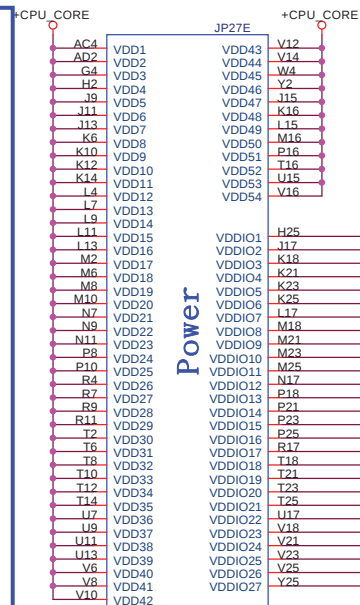
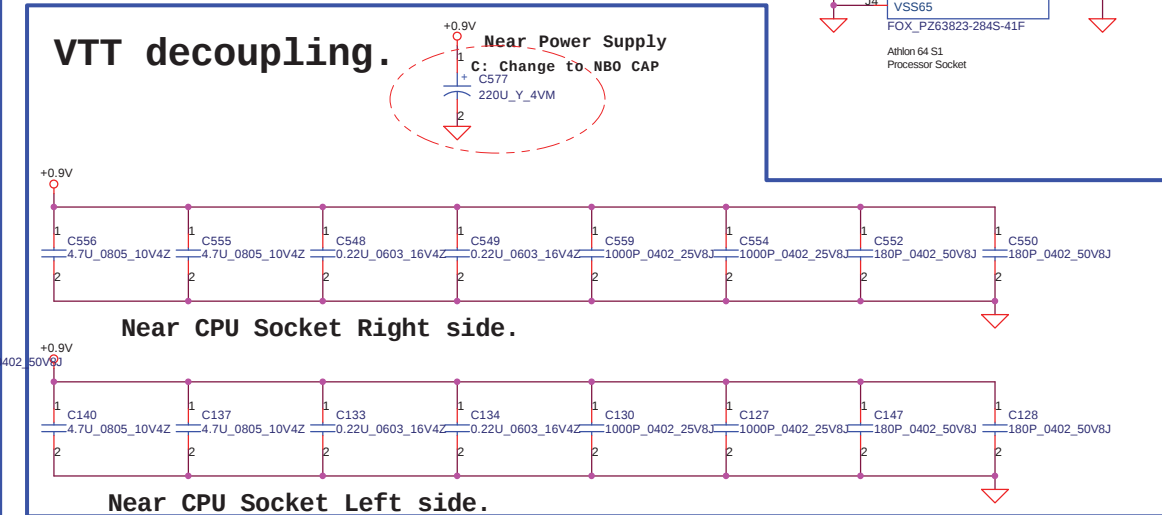
VDD(+CPU_CORE) decoupling.



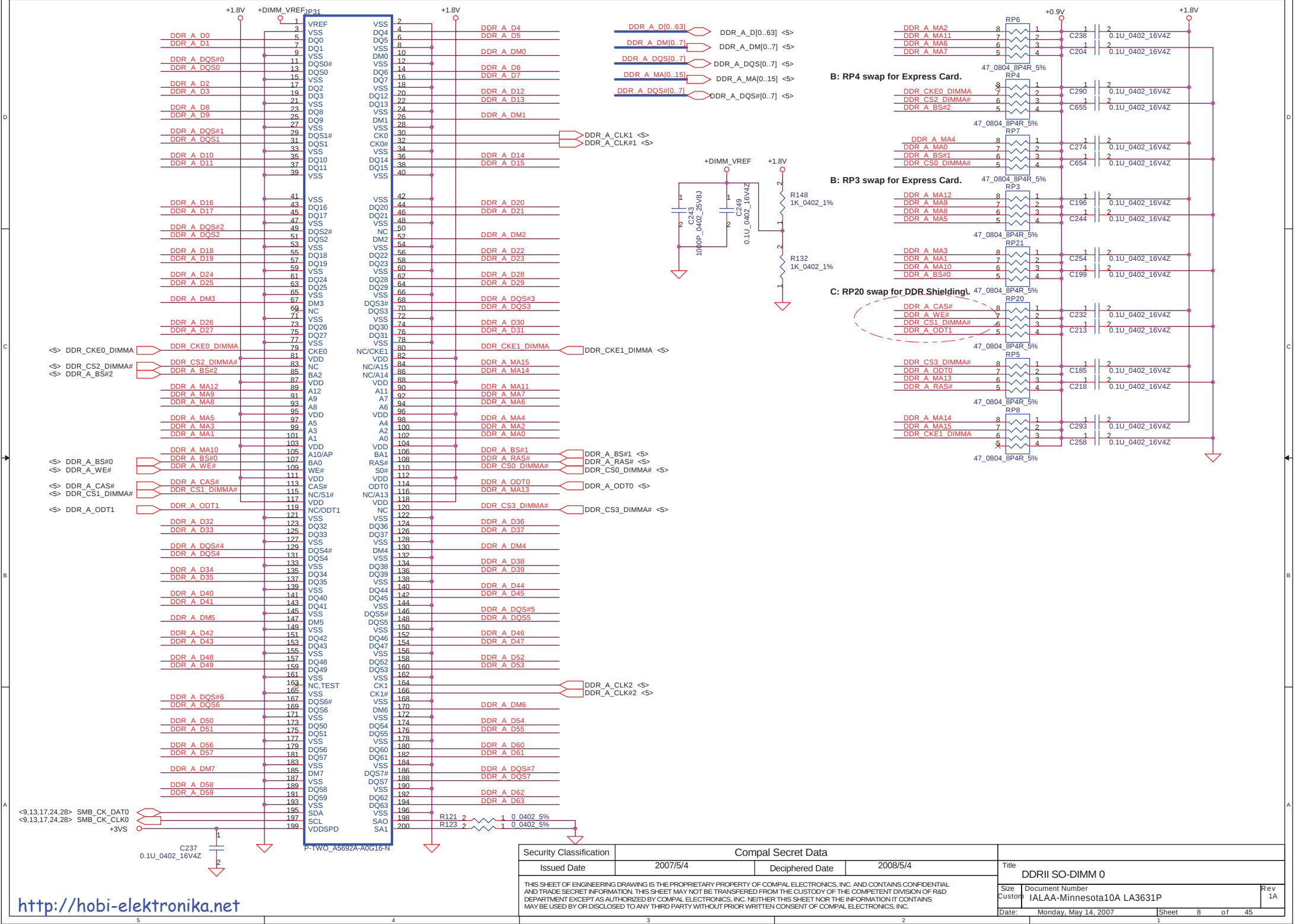
VDDIO decoupling.

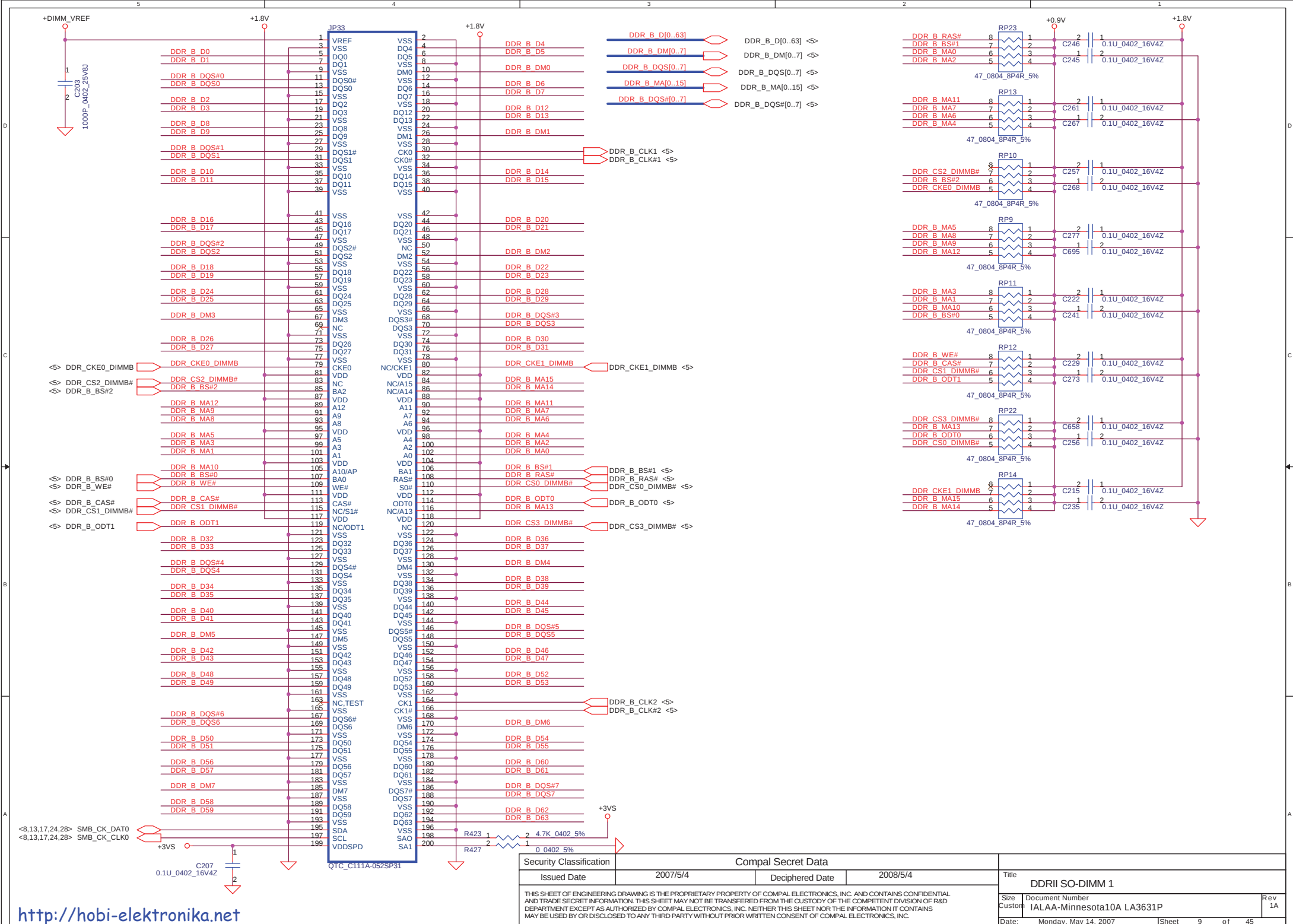


VTT decoupling.

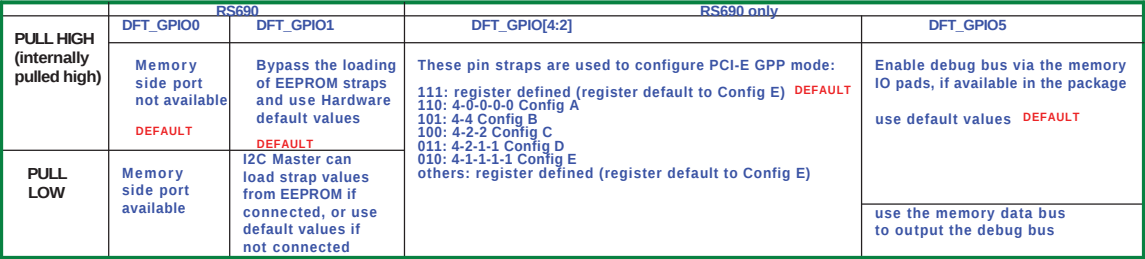


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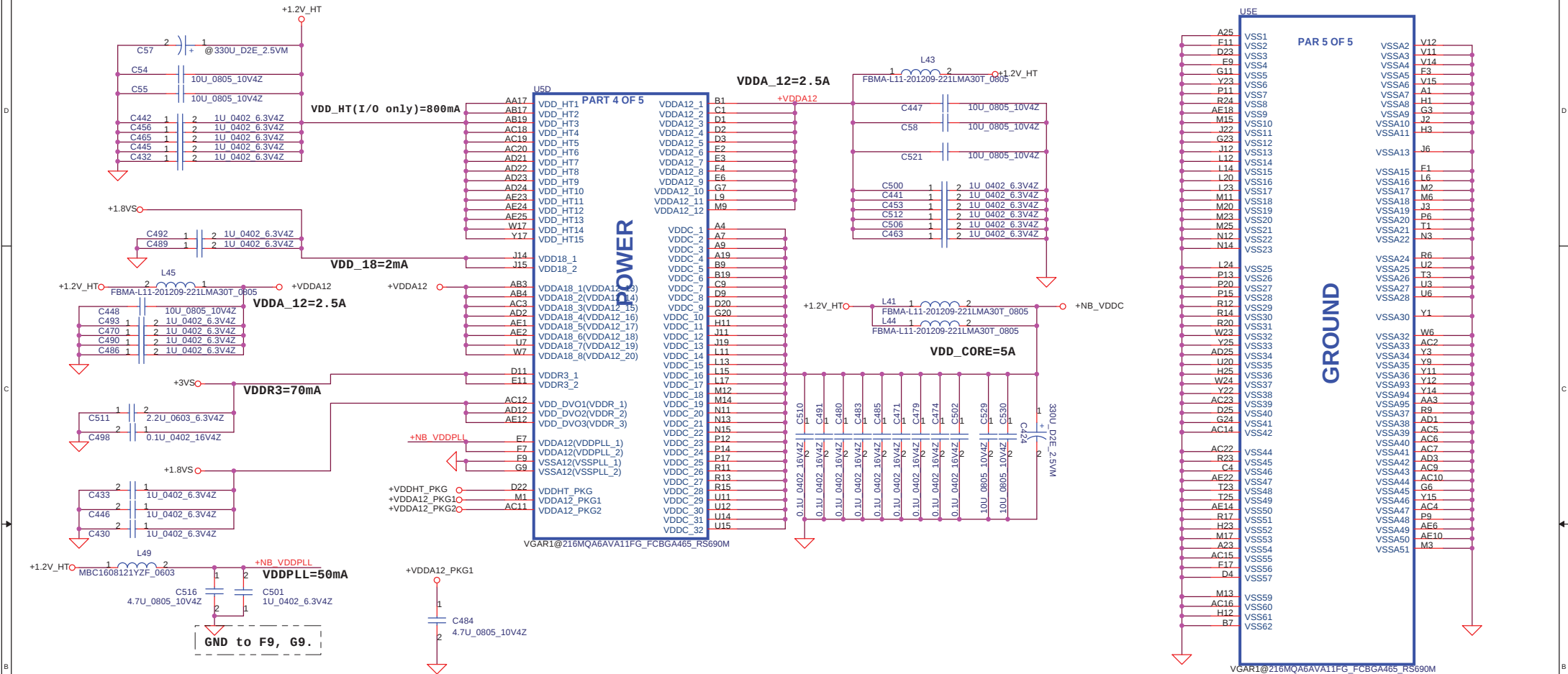


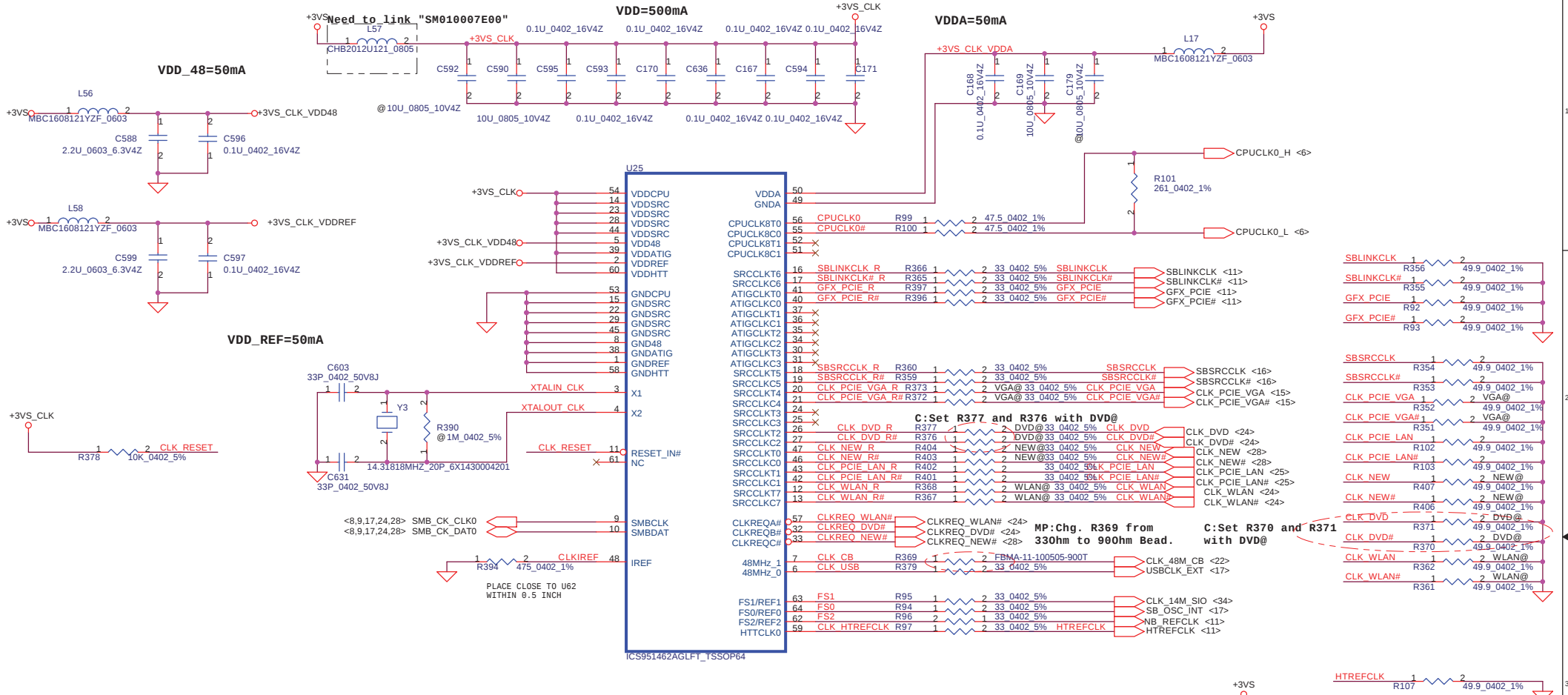


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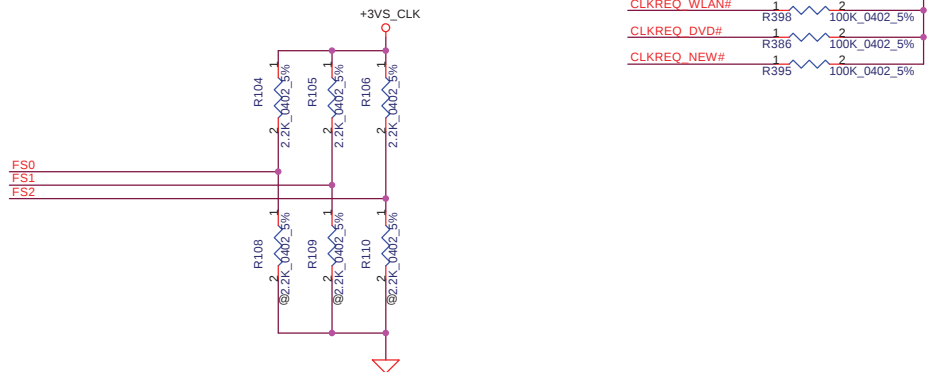
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Issued Date	2007/5/4	Deciphered Date	2008/5/4	RX690/RS690MC Power/GND	
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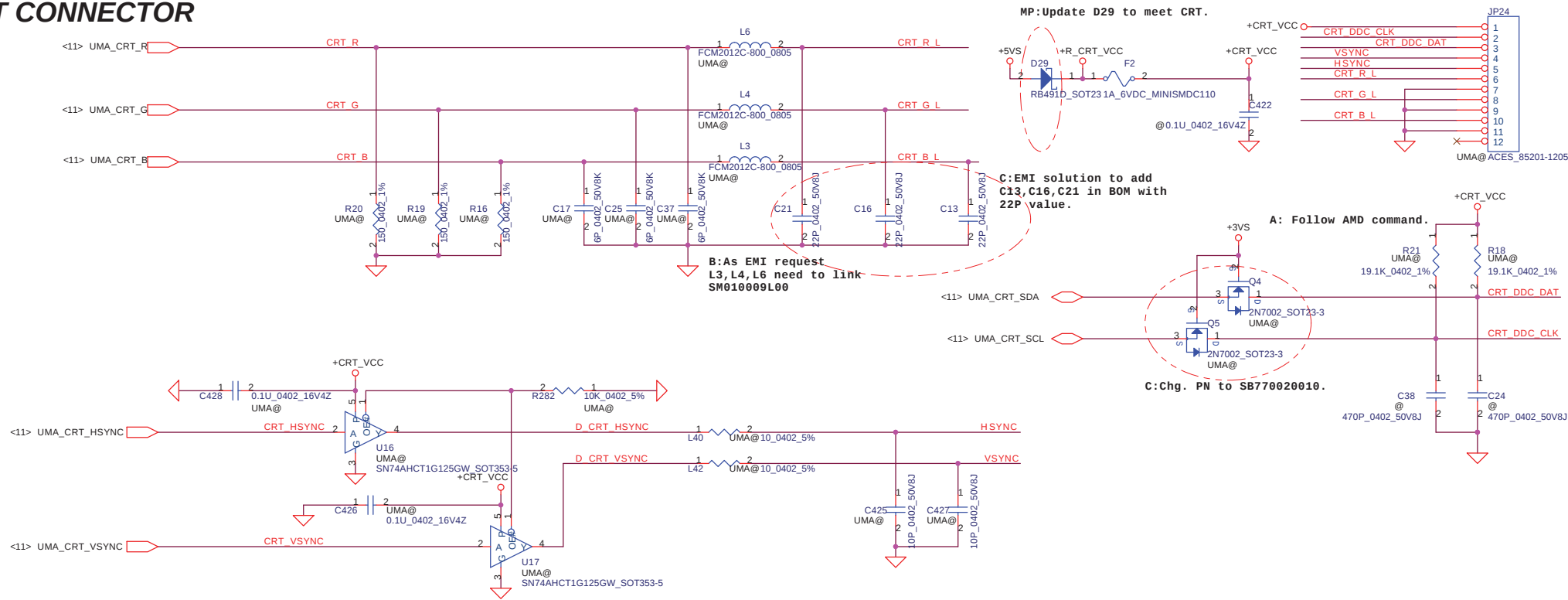
EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

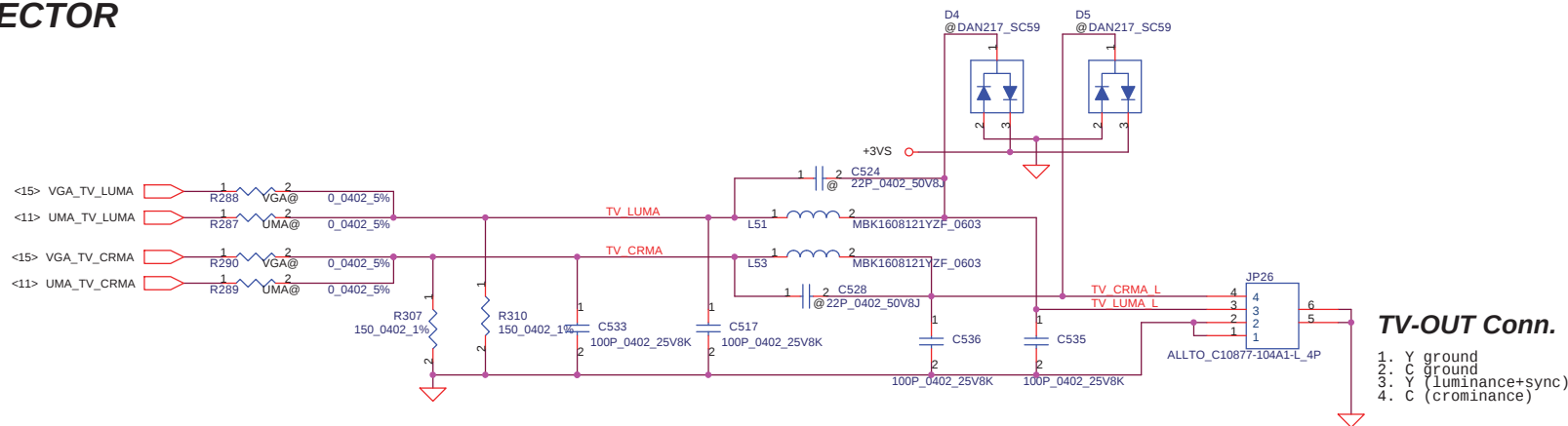


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CRT CONNECTOR



TV-OUT CONNECTOR



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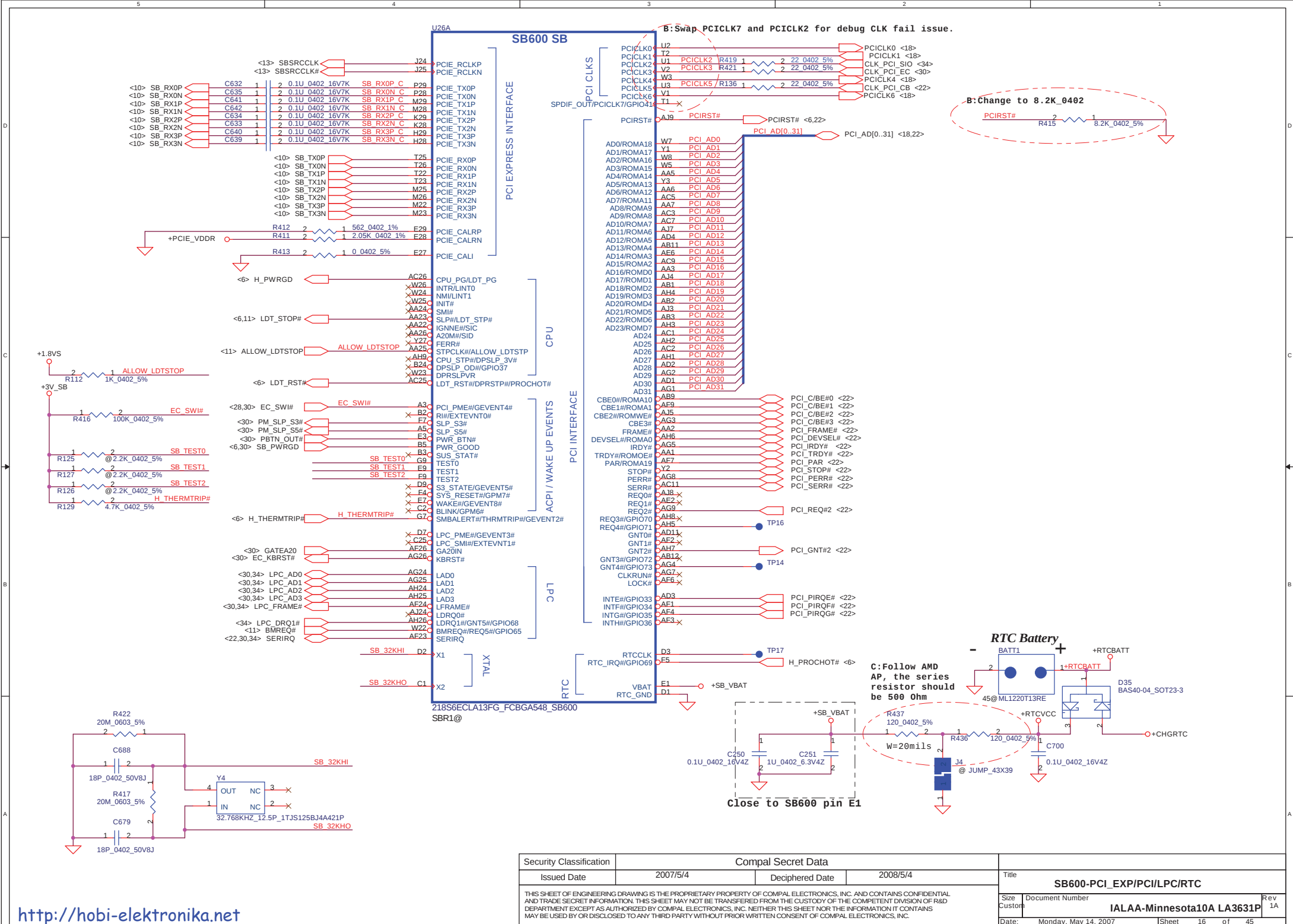
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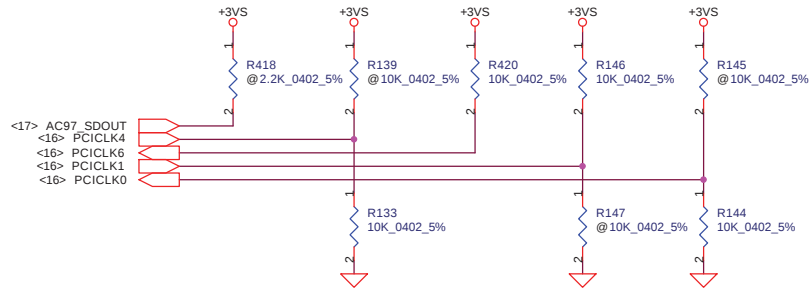
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				SB600-PCI_EXP/PCI/LPC/RTC	
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Standard Straps



Debug Straps



	AC_SDOUT	PCI_CLK4 <PCICLK4>	PCI_CLK6 <PCICLK6>	PCI_CLK1 <CLK_PCI_LAN>	PCI_CLK0 <PCICLK0>
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=AMD DEFAULT	ROM TYPE: H, H = Reserve H, L = LPC ROM L, H = SPI ROM L, L = FWH ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS <int'l PD> DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=Intel		

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 <A11 only>
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE BOOTFAIL TIMER DEFAULT
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	ENABLE BOOTFAIL TIMER

Un-Used Inputs Setting--GPIO pins

GPIO4/SMARTVOLT/SATA_IS2#	Config. GPIO to Output Mode.
GPIO5/SHUTDOWN#	Config. GPIO to Output Mode.
GPIO7/WD_PWRGD	Config. GPIO to Output Mode.
GPIO8/DDC1_SDA	Config. GPIO to Output Mode.
GPIO9/DDC1_SCL	Config. GPIO to Output Mode.
GPIO10/SATA_IS0#	Config. GPIO to Output Mode.
GPIO41/PCICLK7/SPDIF_OUT	Config. GPIO to Output Mode.
GPIO50/FANIN0	Config. GPIO to Output Mode.
GPIO51/FANIN1	Config. GPIO to Output Mode.
GPIO52/FANIN2	Config. GPIO to Output Mode.
GPIO53/VIN0	Config. GPIO to Output Mode.
GPIO54/VIN1	Config. GPIO to Output Mode.
GPIO55/VIN2	Config. GPIO to Output Mode.

Un-Used Inputs Setting--GPM pins

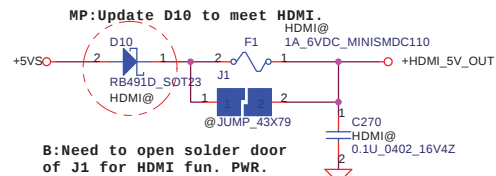
GPIO56/VIN3	Config. GPIO to Output Mode.
GPIO57/VIN4	Config. GPIO to Output Mode.
GPIO58/VIN5	Config. GPIO to Output Mode.
GPIO59/VIN6	Config. GPIO to Output Mode.
GPIO60/VIN7	Config. GPIO to Output Mode.
GPIO61/TEMPIN0	Config. GPIO to Output Mode.
GPOC2#SCL1	Config. GPIO to Output Mode.
GPOC3#SDA1	Config. GPIO to Output Mode.

Un-Used Inputs Setting--GPM pins

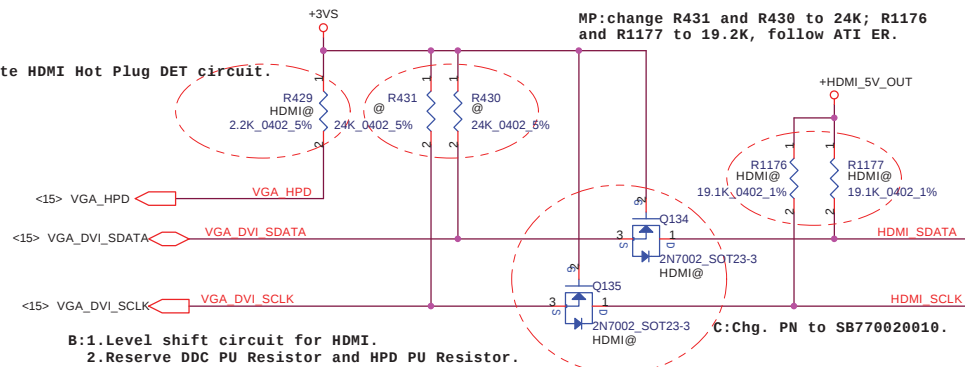
GPM5#/DDR3_RST#/USB_OC5#	Config. for internal PU.
GEVENT5#S3_STATE	Config. for internal PU.

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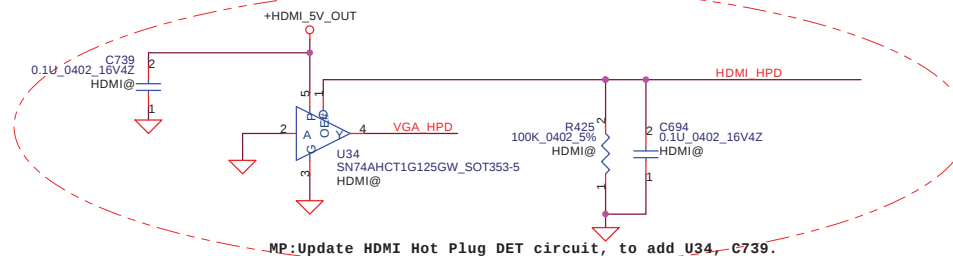
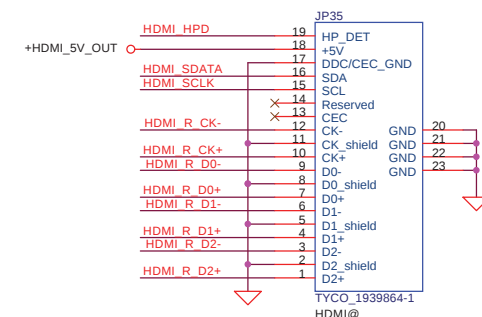
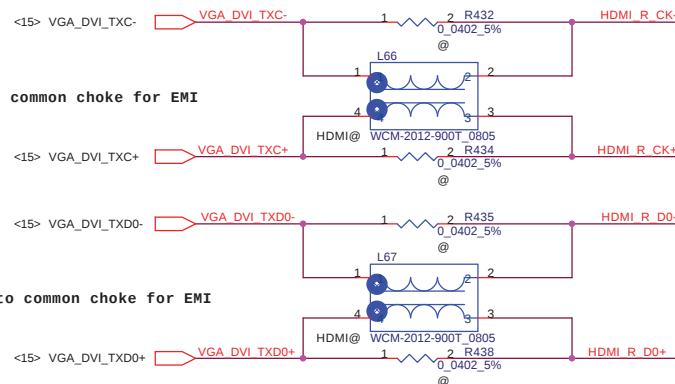
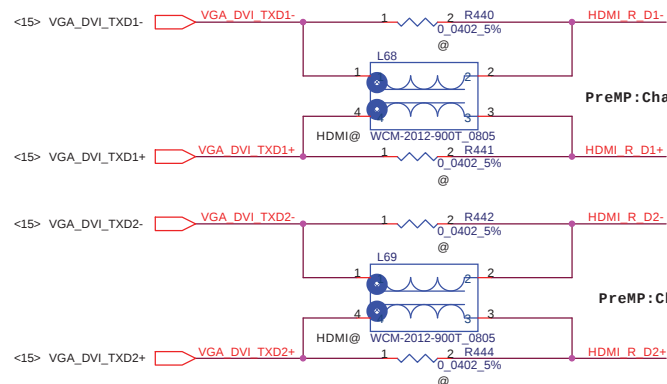
B:Remove HDMI transistor, SiI1932; and support by GPU only.



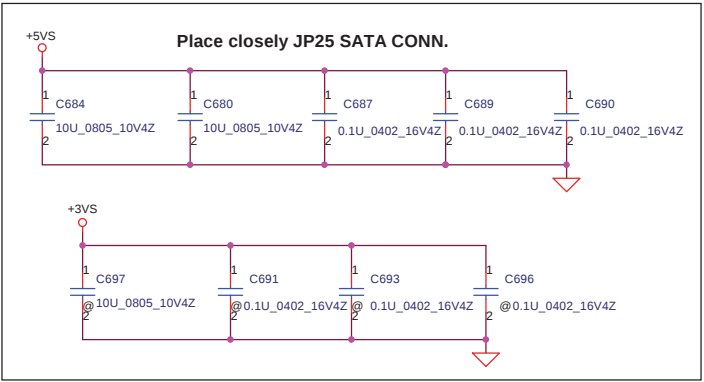
MP:Update HDMI Hot Plug DET circuit.



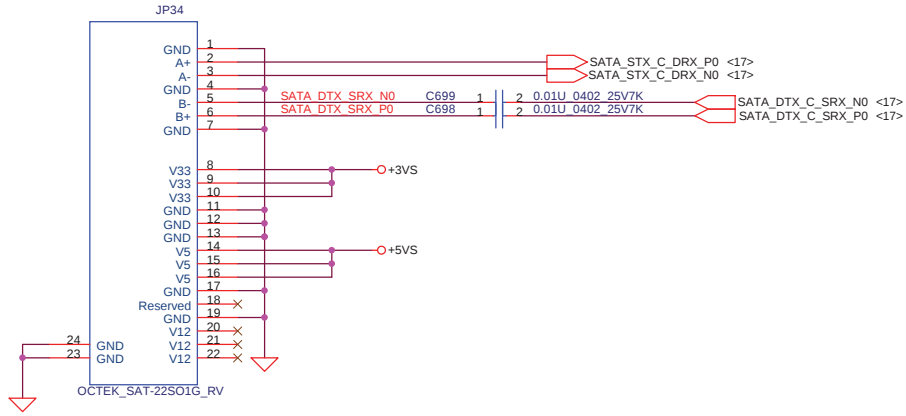
HDMI Connector



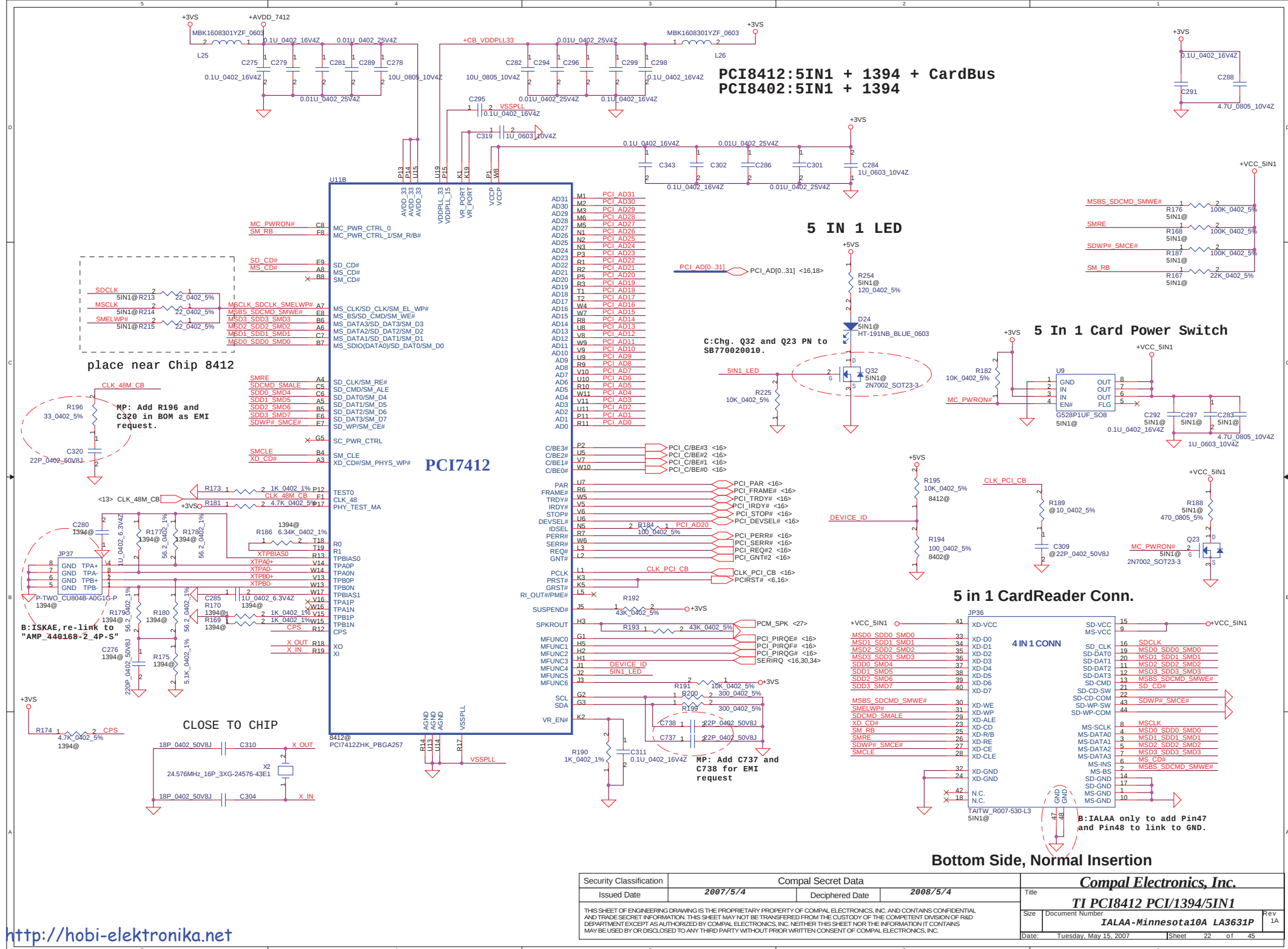
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SATA HDD Conn.



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PCI8412:5IN1 + 1394 + CardBus
PCI8402:5IN1 + 1394

5 IN 1 LED

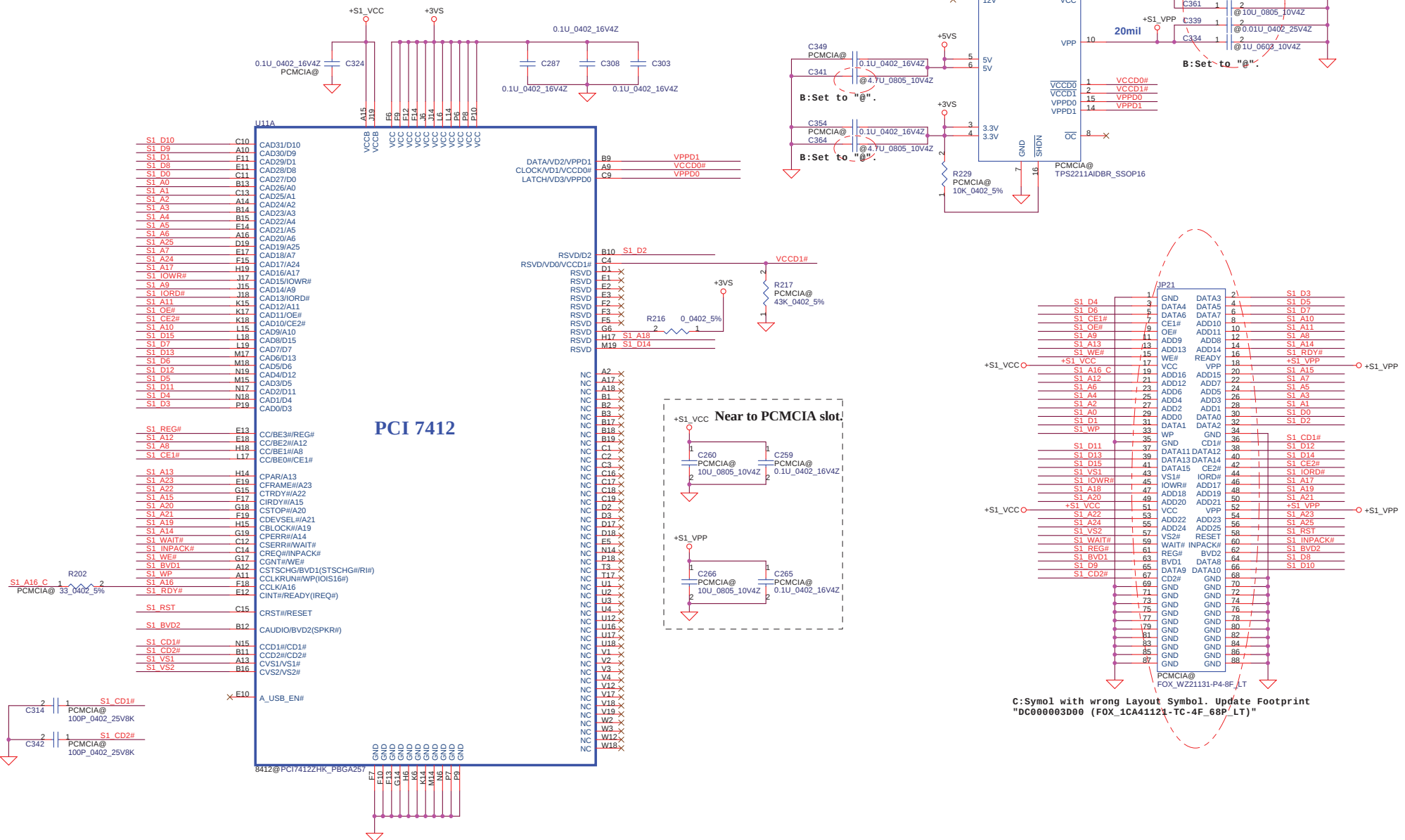
5 In 1 Card Power Switch

5 in 1 CardReader Conn.

Bottom Side, Normal Insertion

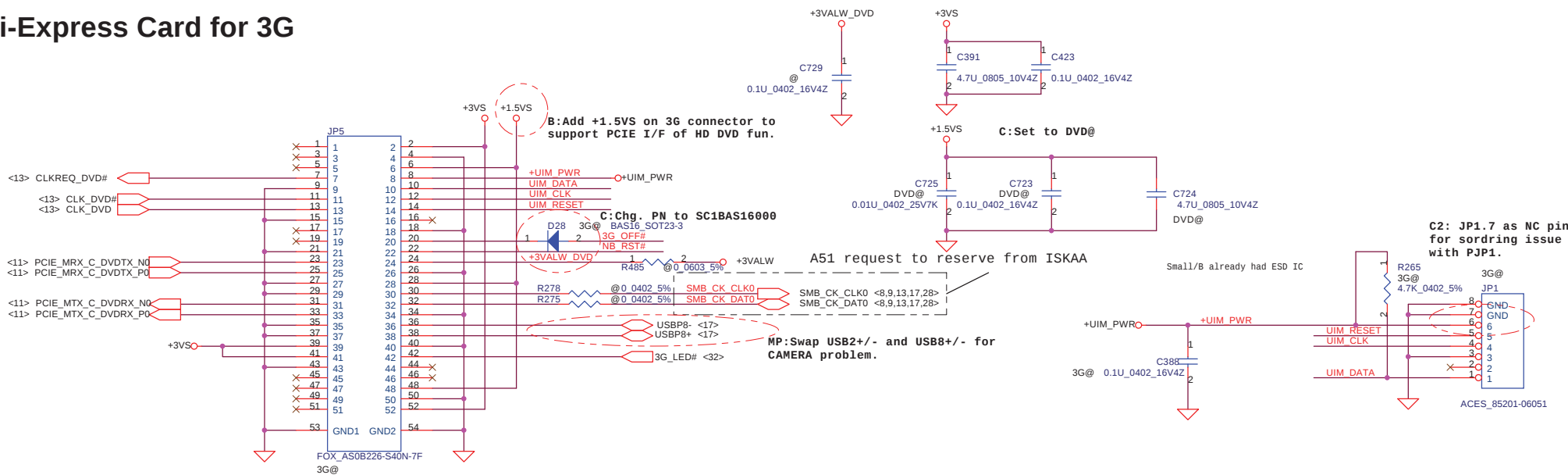
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CardBus Power Switch

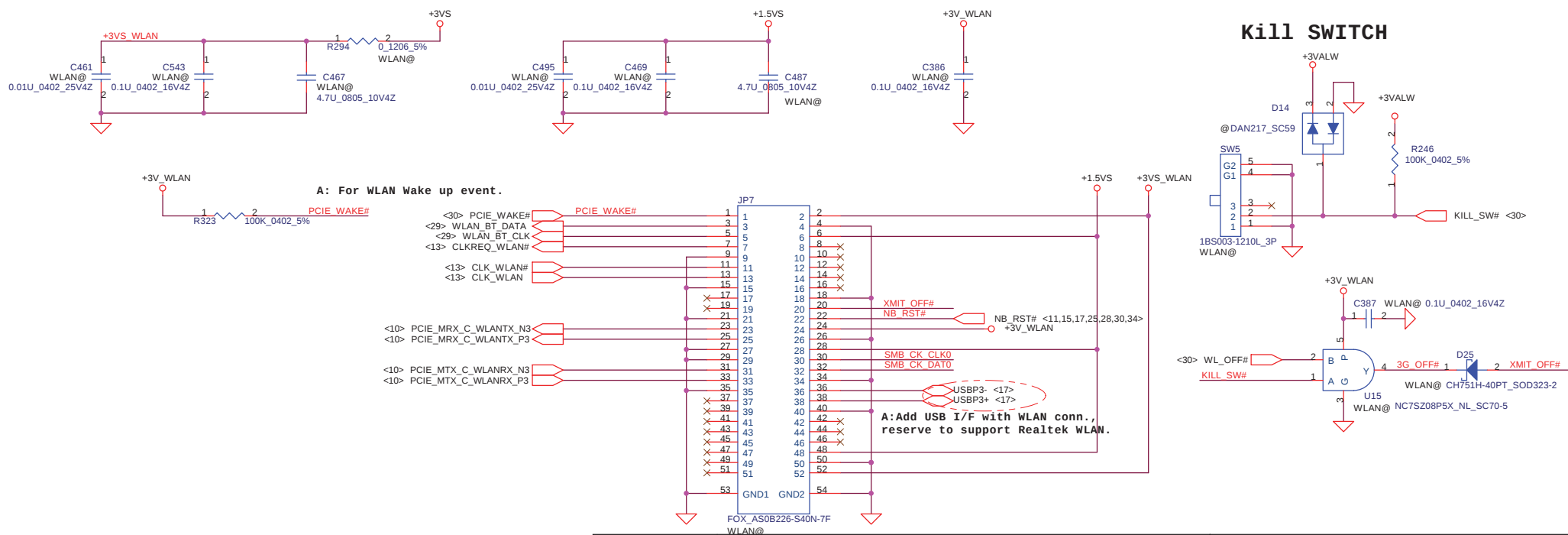


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Mini-Express Card for 3G



Mini-Express Card for WLAN



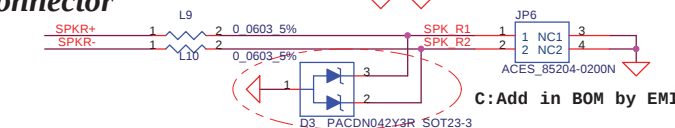
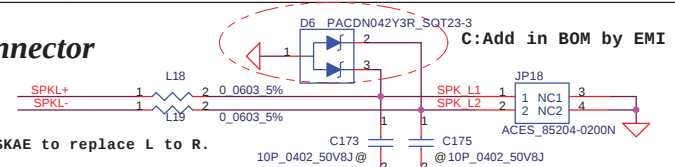
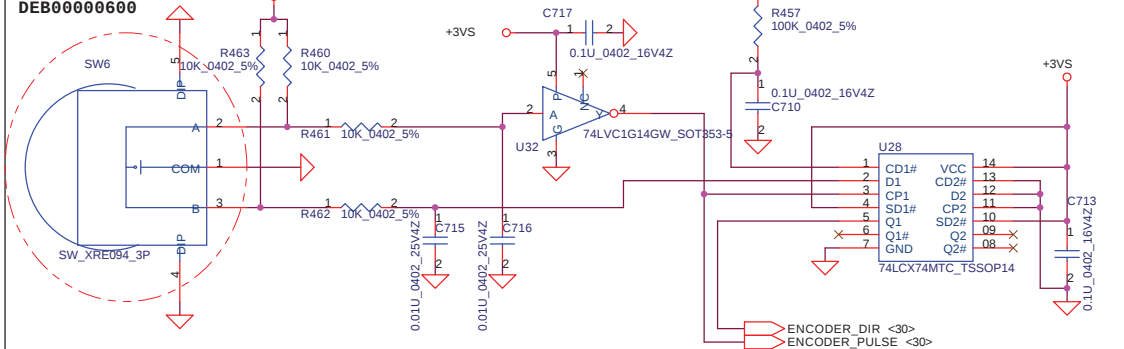
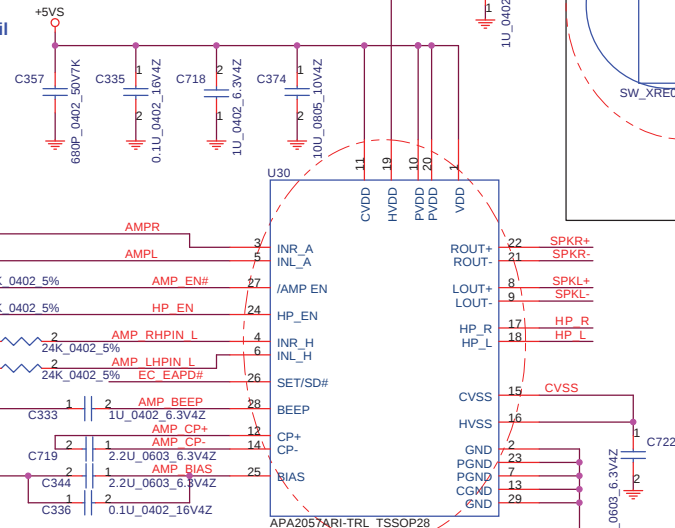
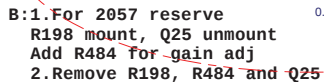
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Issued Date		Deciphered Date		Title	
2007/5/4		2008/5/4		MINI PCI SLOT	
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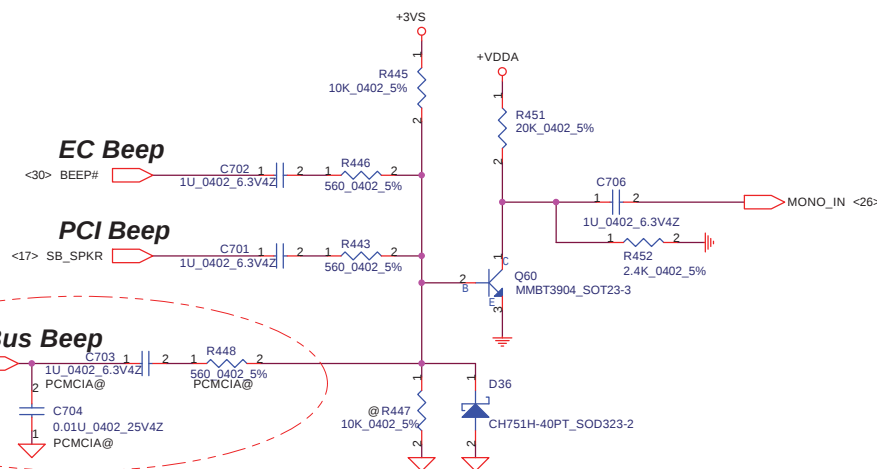
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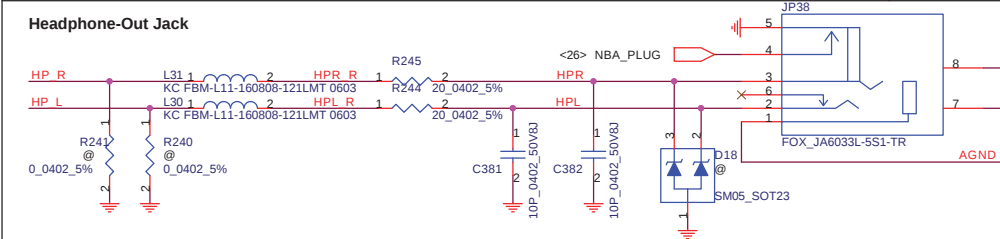
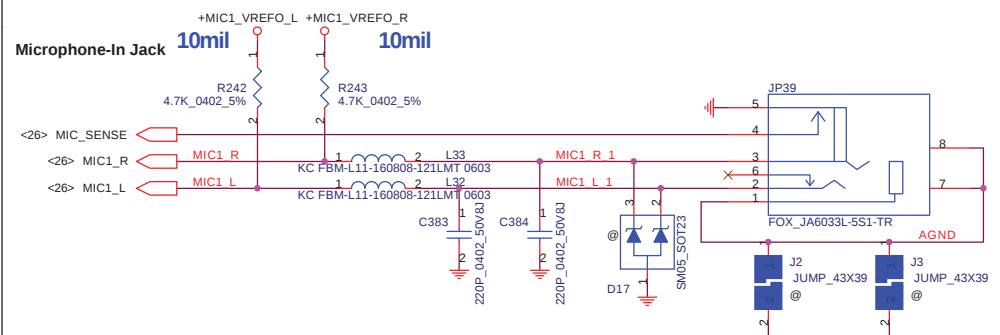
1



Gain	HP	0dB
	SPK	10dB

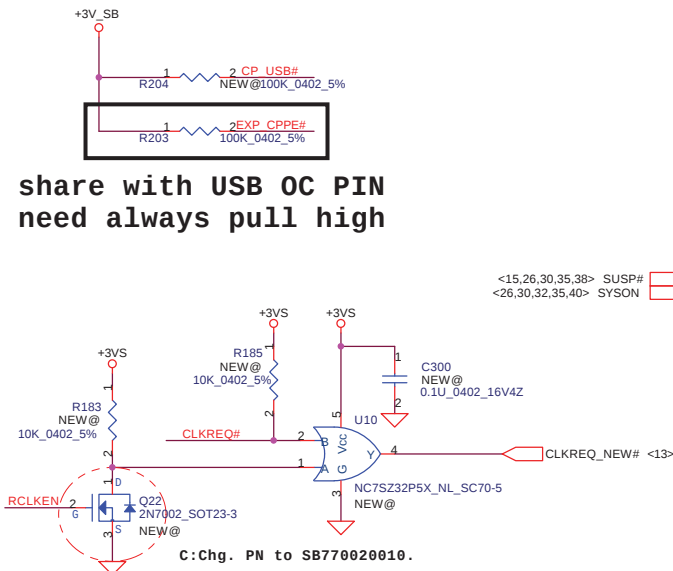
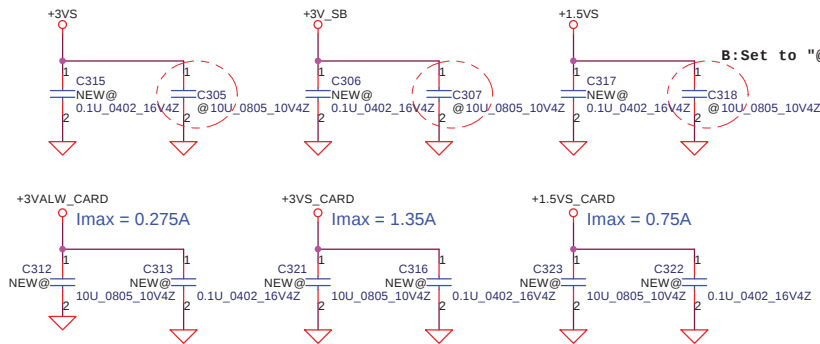
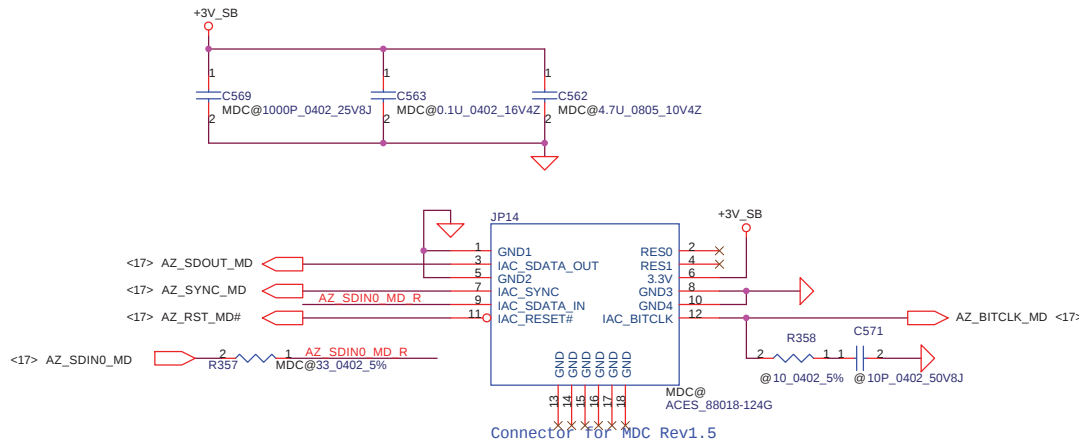


```
A:Set PCMCIA@ on CardBus Beep circuit
B:Remove NSE_DPR circuit, bec'z chg. to KB926.
```



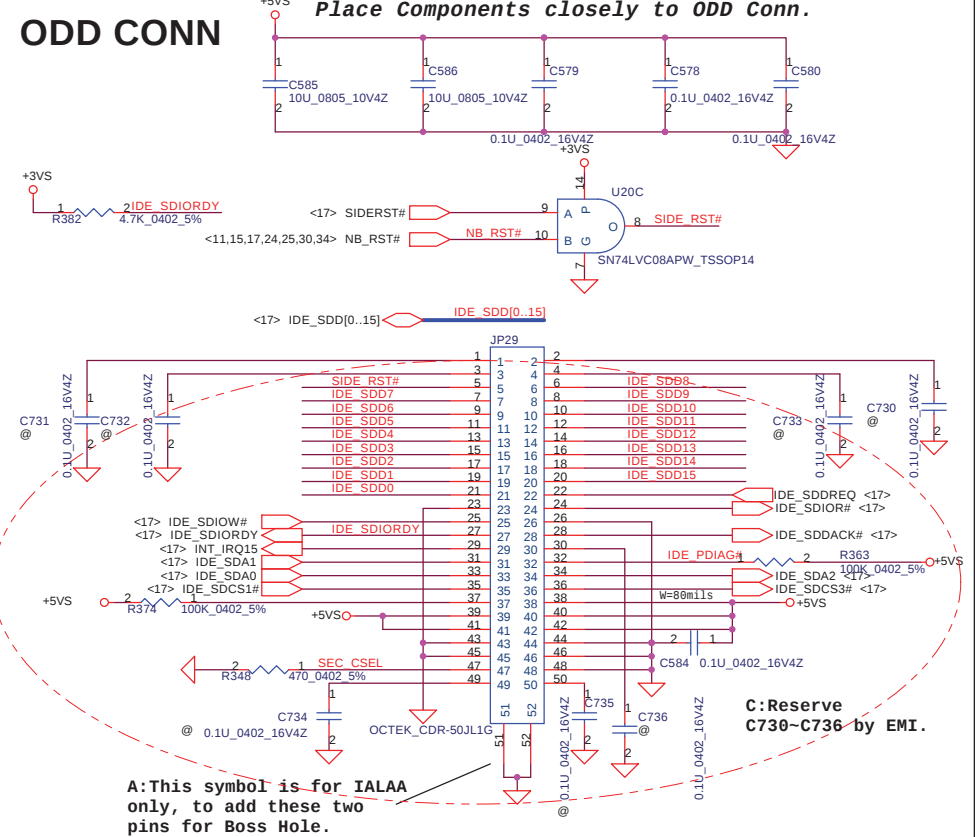
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Issued Date		2007/5/4	Deciphered Date	2008/5/4		Title
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				Size	Document Number	Rev
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MDC 1.5 Conn.

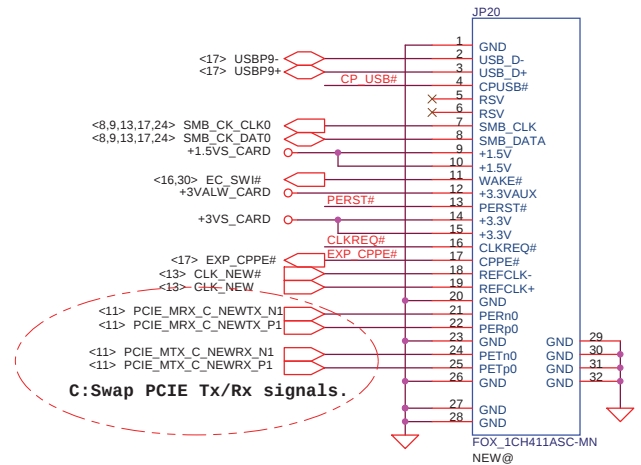


ODD CONN

Place Components closely to ODD Conn.



B: relink DC030006000.



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Check 5VS or 3VS



Fingerprint Conn

CIR



Bluetooth Interface

C:Chg. PN to SB770020010.

Pull high at SB600 side

Module ID

Indication for polarity of reset

Reset input High Active --> Low ,

Reset input Low Active --> Open

B:Add PD 4.7K bec'z chg. to KB926.

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USB CONN. 1**USB CONN.2**

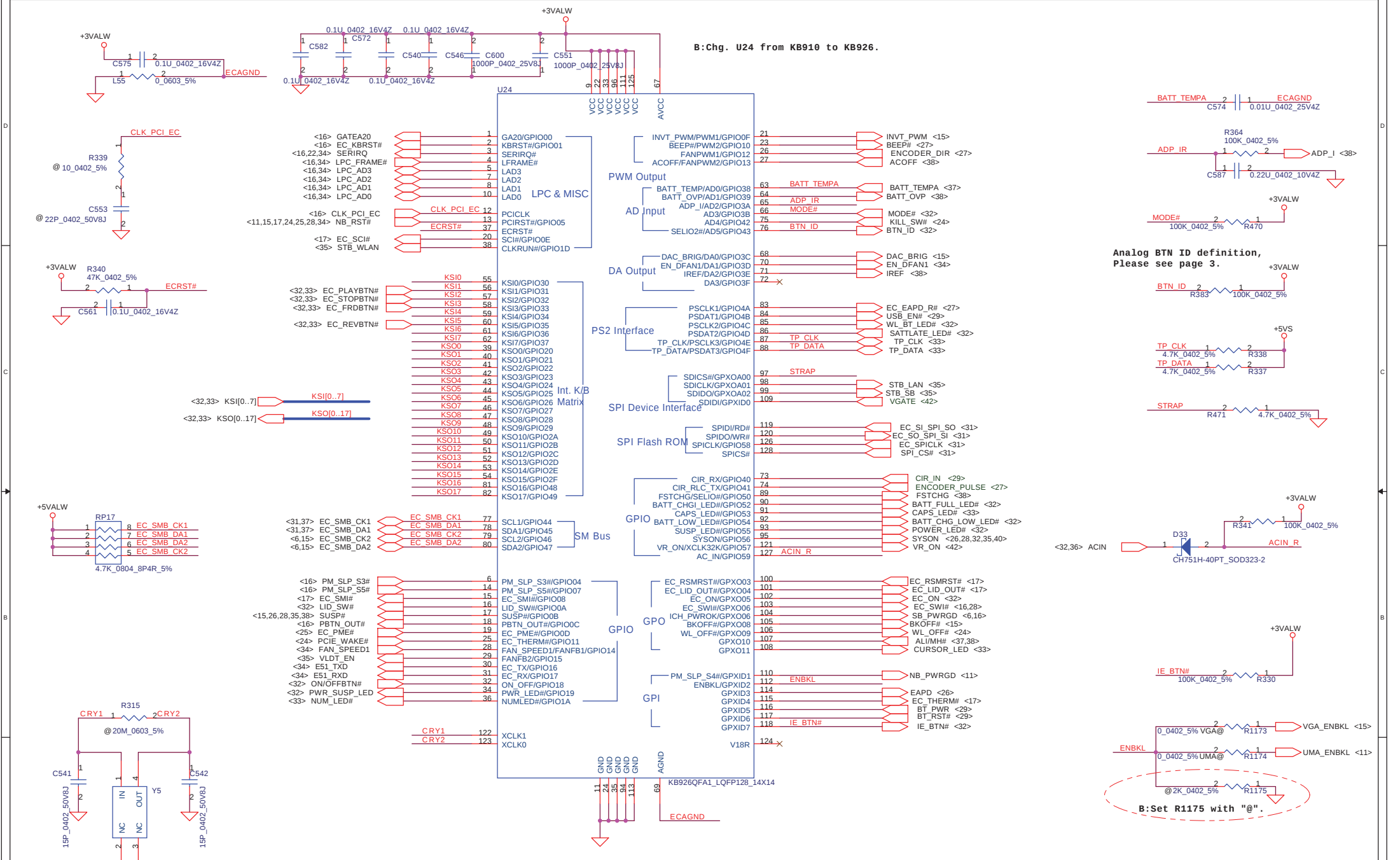
USB Small Board



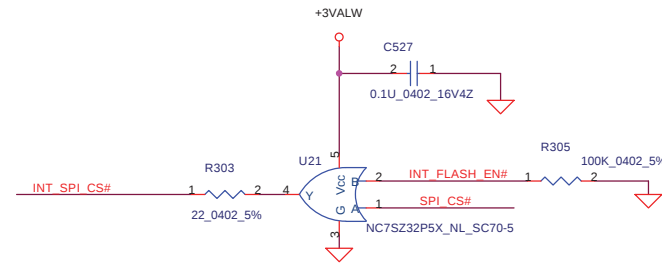
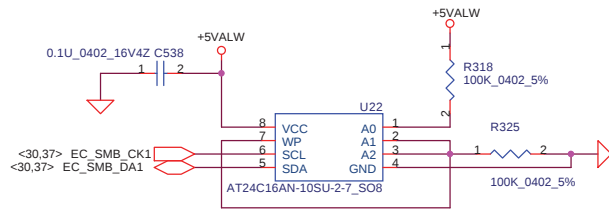
MP:Swap USB2+/- and USB8+/- for CAMERA problem.

USB Conn.

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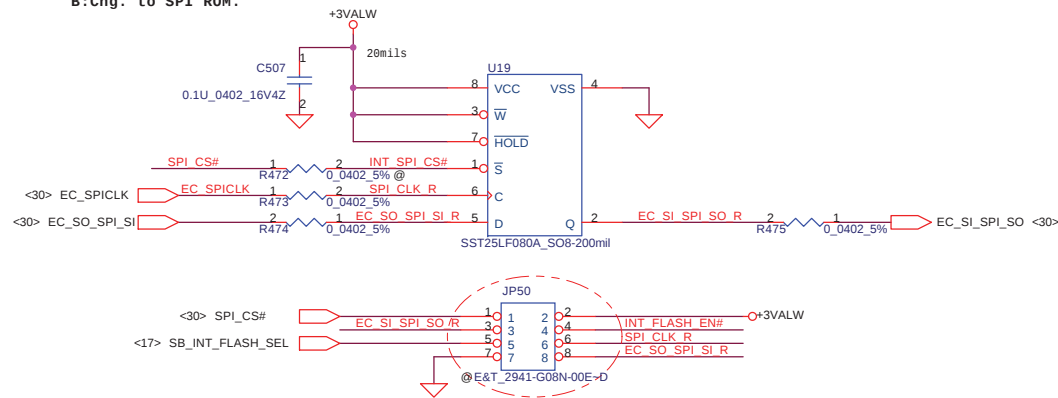


32.768KHZ_12.5P 17JS125BJ4A421P
MP:ENE's recommend, change C541 and C542 from 10P to 27P.
MP:ENE's recommend, change back C541 and C542 from 27P to 15P.



SPI Flash (8Mb*1)

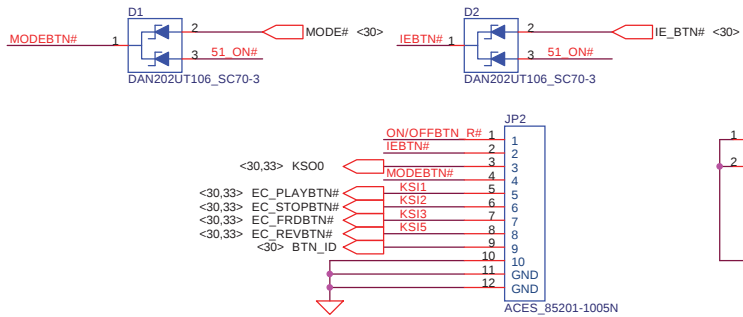
B:Chg. to SPI ROM.



C:Chg. PN to LTC00000200

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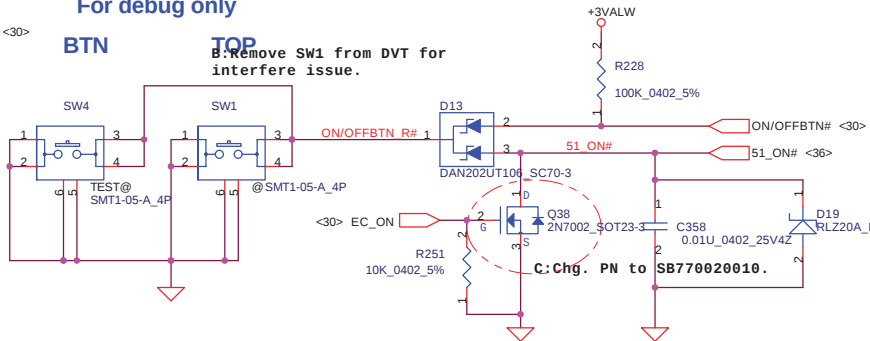
SW/LED Connector



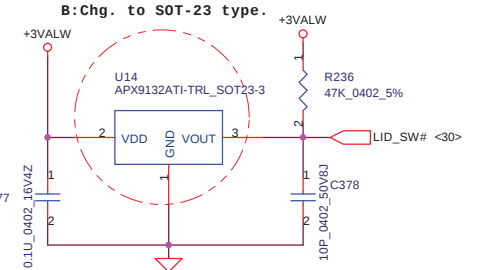
Power Button

For debug only

BTN



Lid SW

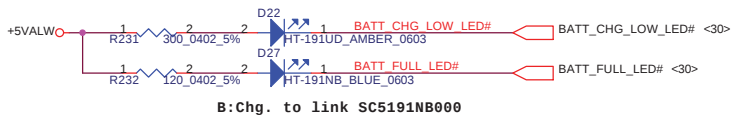


AC IN LED

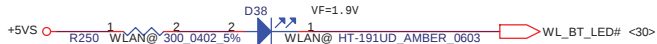
B:Chg. to link SC5191NB000



BATT CHARGE/FULL LED

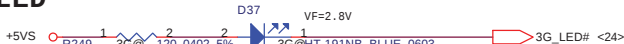


WL&BT LED



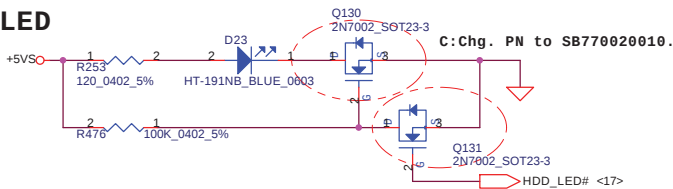
3G LED

B:Chg. to link SC5191NB000

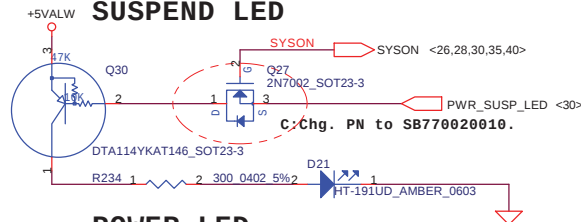


HDD LED

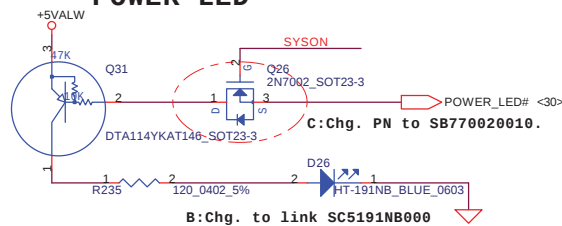
B:Chg. HDD LED control circuit bec'z chg. to KB926.



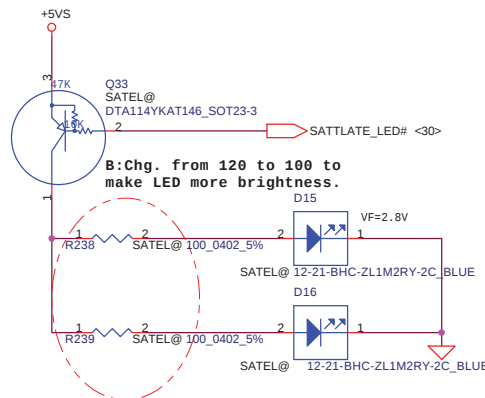
SUSPEND LED



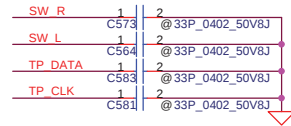
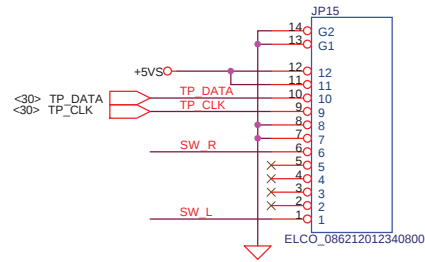
POWER LED



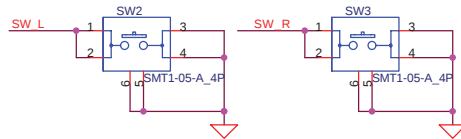
Satellite LED



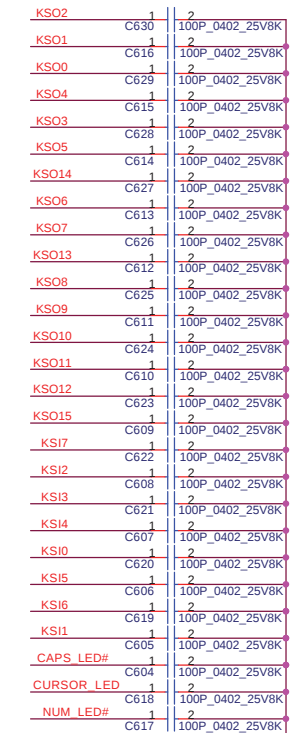
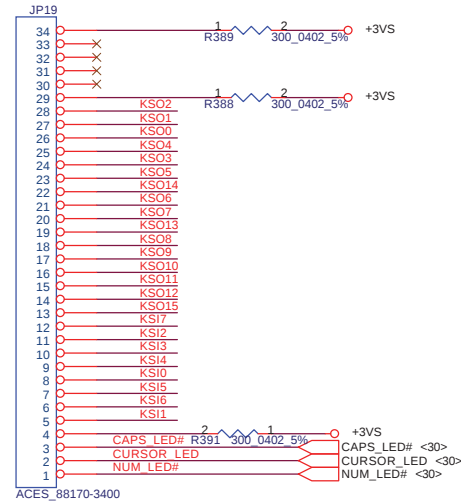
TP Conn.



TP Button



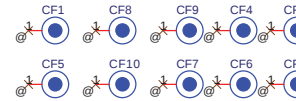
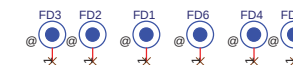
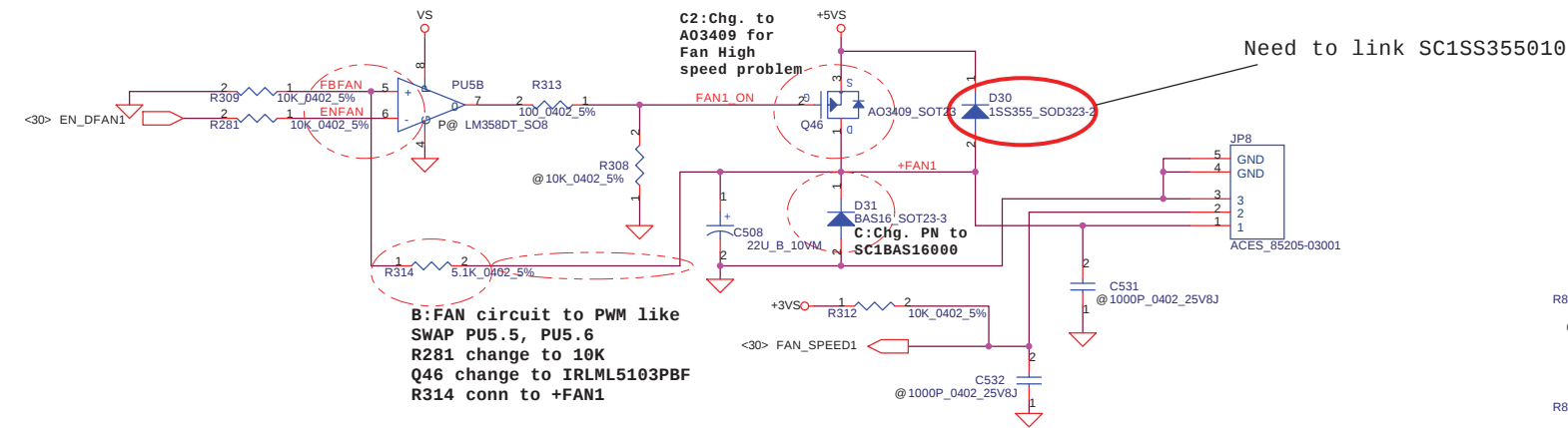
KEYBOARD CONN.



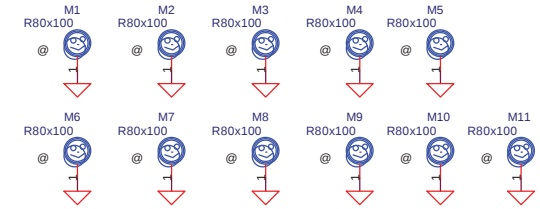
For EMI Request

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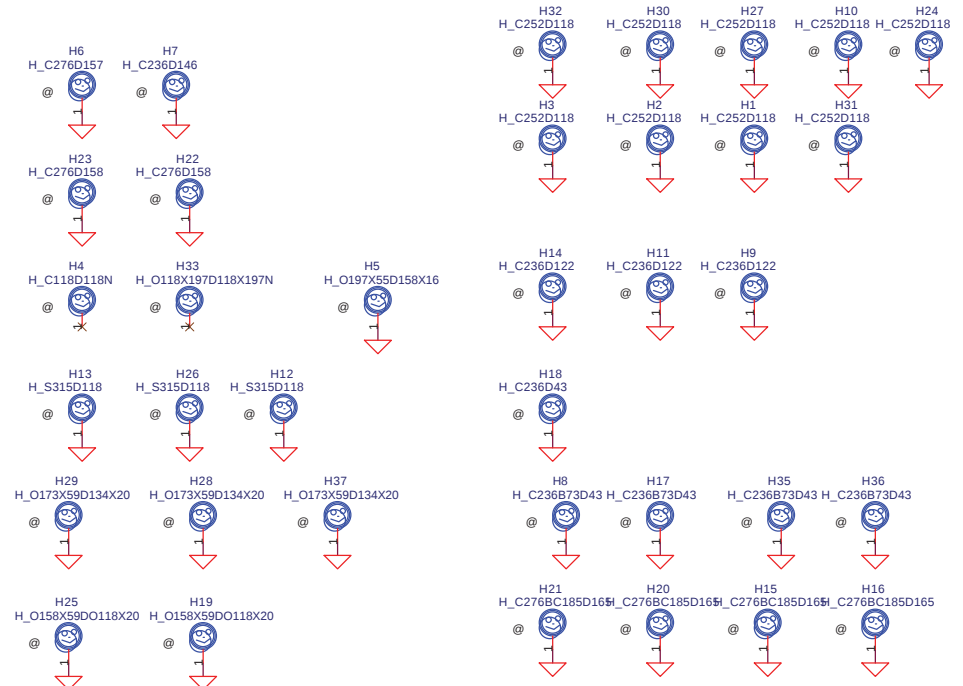
FAN Conn



EMI Shielding Clip PADS

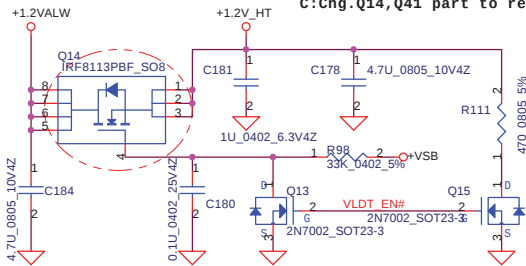


Screw Hole

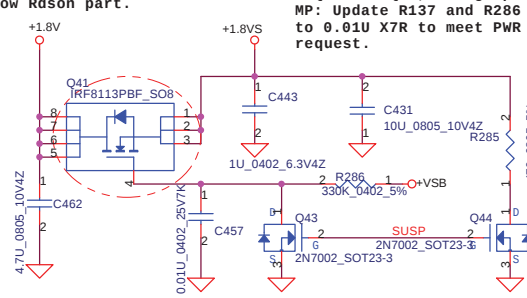


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+1.2VALW TO +1.2V_HT

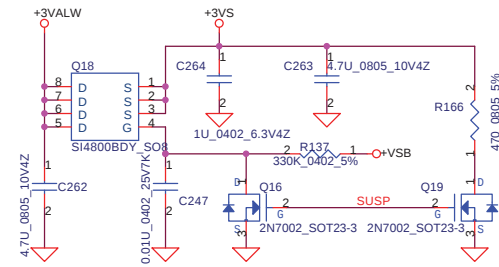


+1.8V TO +1.8VS

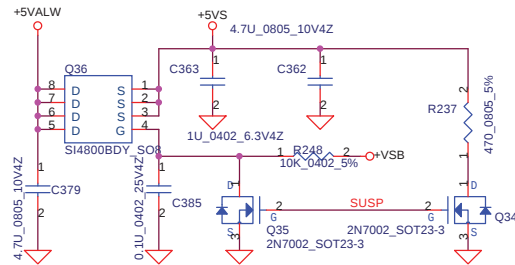


B:Q18 and Q36, need to link "SB548000310"
C:Q14 and Q41, change part to reduce Rds(on) to improve PWR drop.
MP: Update R137 and R286 from 22K to 330K and C247 and C457 from 0.1U Y5V to 0.01U X7R to meet PWR SEQ, and update C180 and C385 to 25V to meet PWR request.

+3VALW TO +3VS

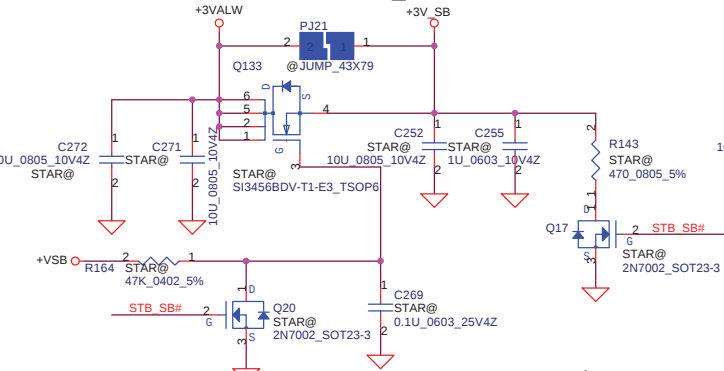


+5VALW TO +5VS

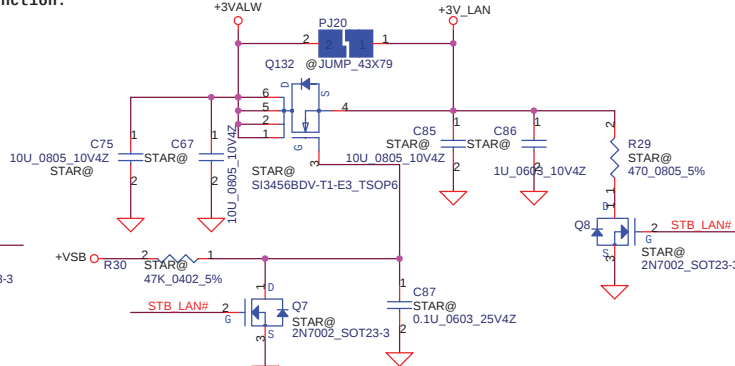


B:Add PD 100K bec'z KB926 is tri-state pin.

+3VALW TO +3V_SB



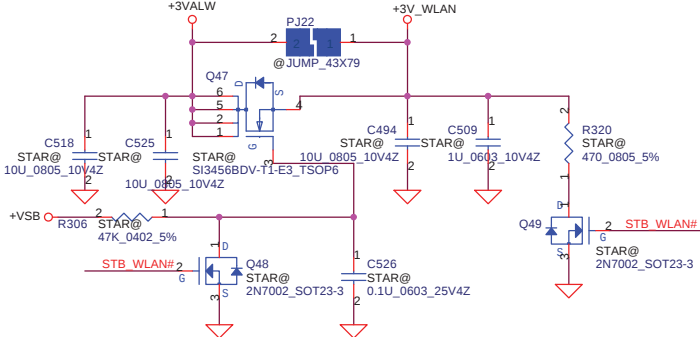
+3VALW TO +3V_LAN



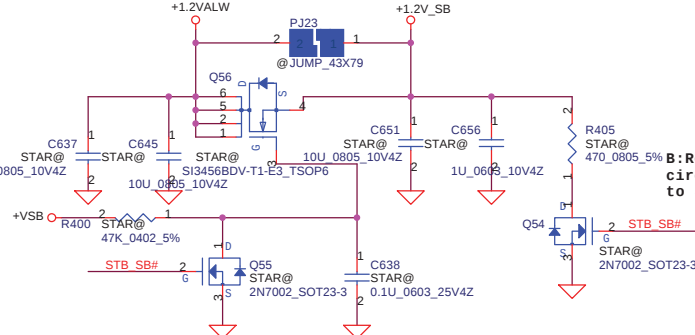
B:Remove Energy Star 4.0 function.

C:Chg. PN to SB770020010.

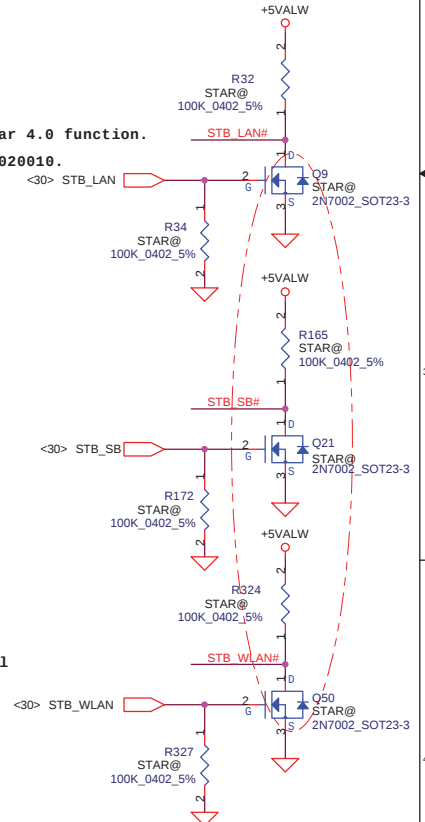
+3VALW TO +3V_WLAN



+1.2VALW TO +1.2V_SB

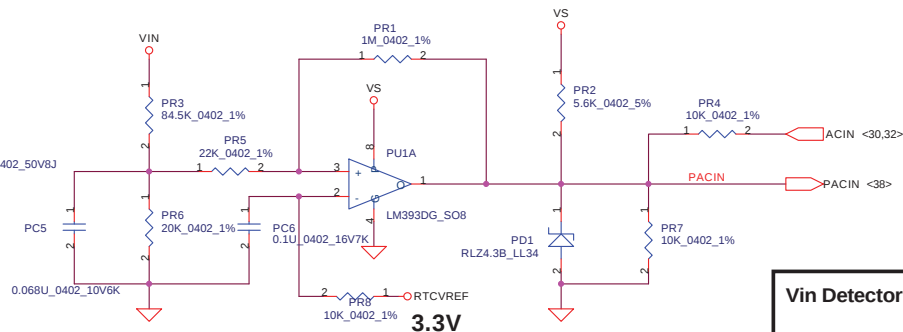
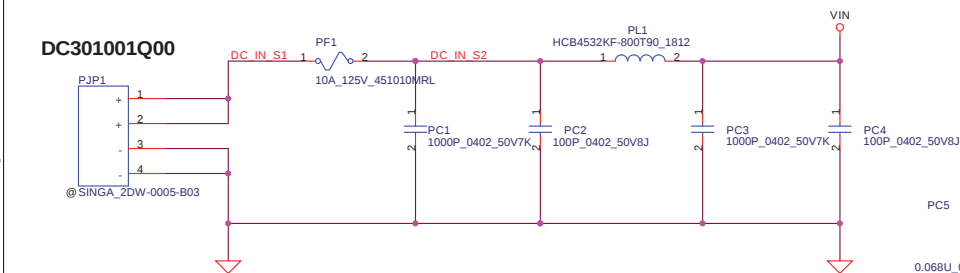


B:Remove STB_12SB# control circuit and chagne control signl to STB_SB#



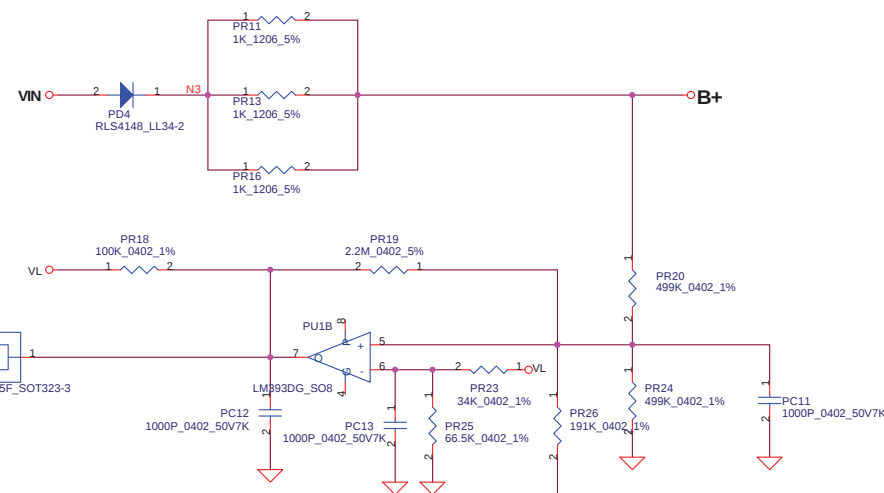
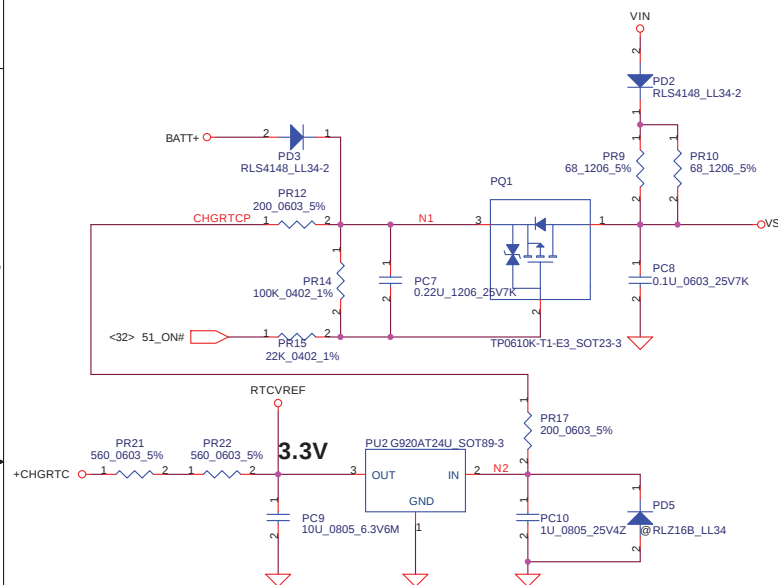
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DC301001Q00

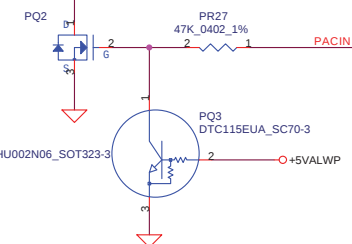


Vin Detector

High 18.384 17.901 17.430
Low 17.728 17.257 16.976



Precharge detector 15.97V/14.84V FOR ADAPTOR



+3VALWP (5A, 200mils, Via NO.= 10)

+5VALWP (5A, 200mils, Via NO.= 10)

+VSBP (120mA, 40mils, Via NO.= 2)

+1.8VP (8A, 320mils, Via NO.= 16)

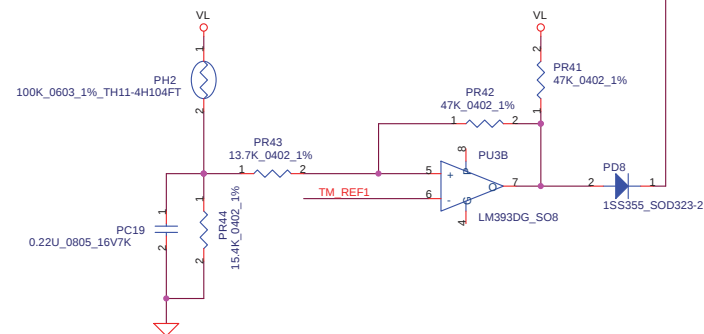
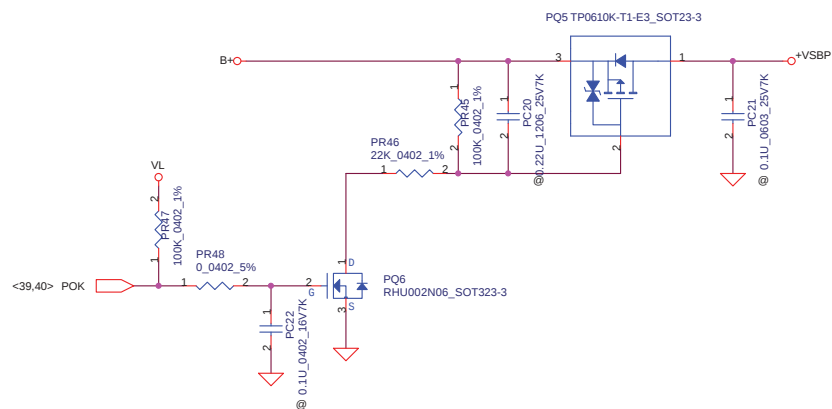
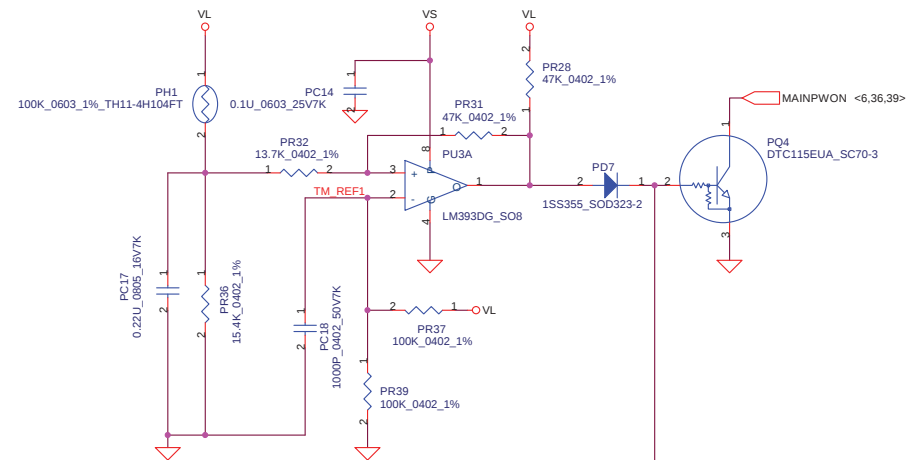
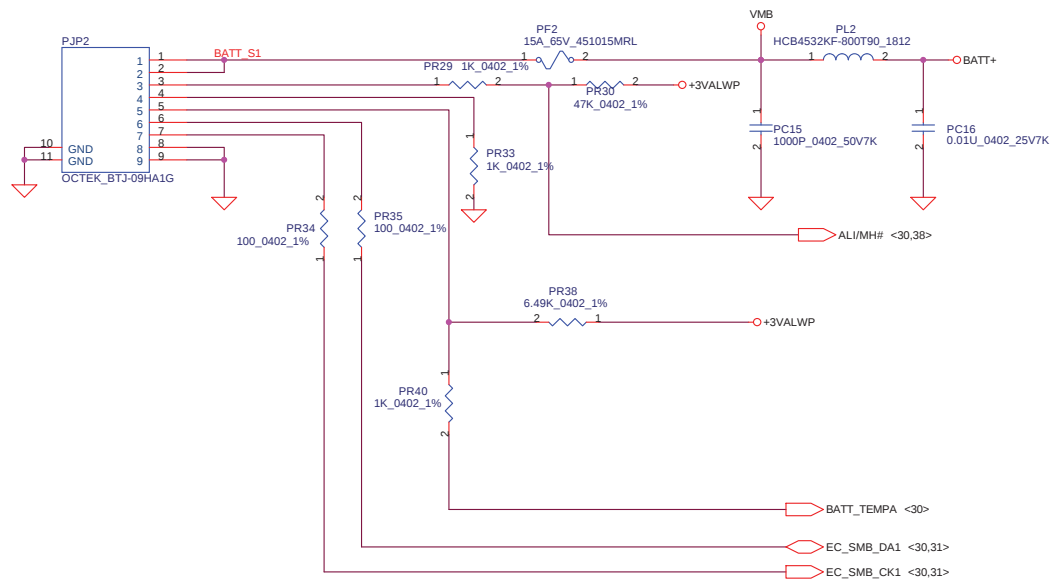
+1.5VSP (3.0A, 120mils, Via NO.= 6)

+0.9VP (2A, 80mils, Via NO.= 4)

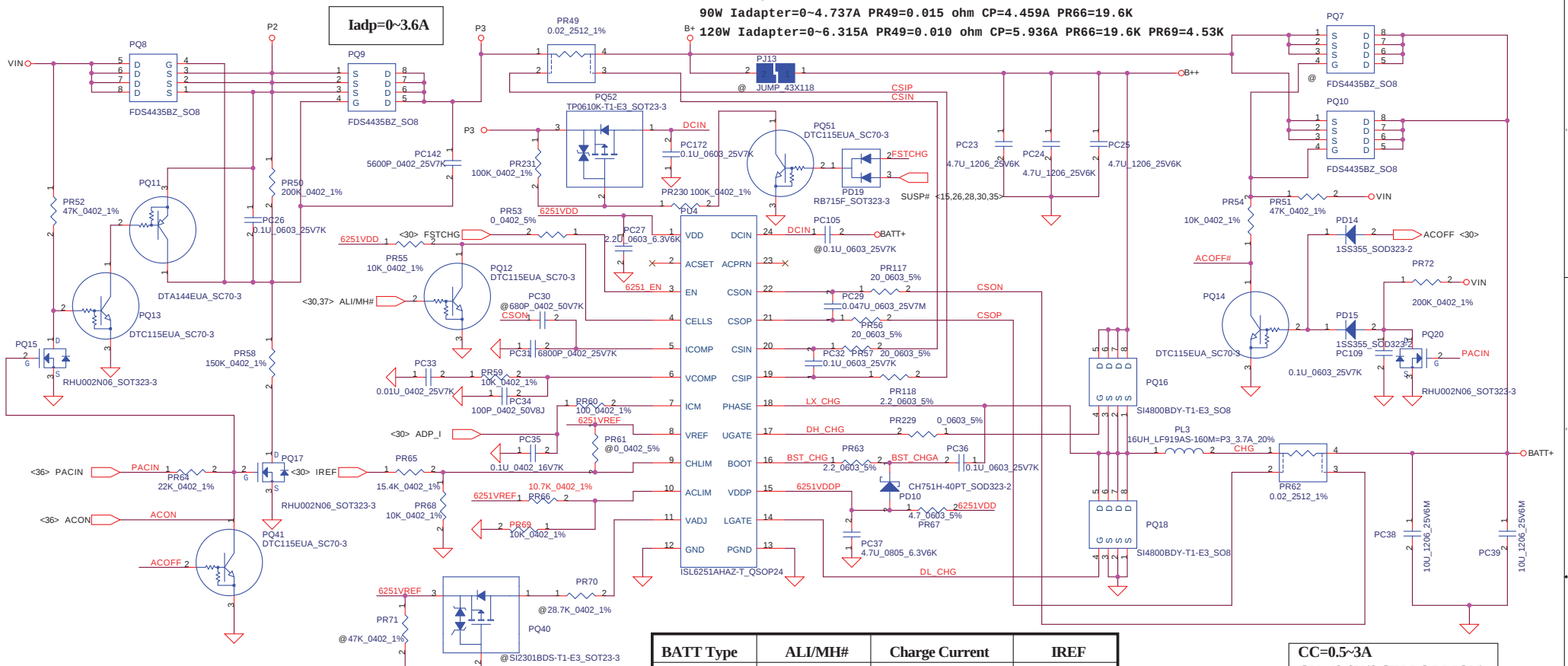
+1.2VALWP (8A, 320mils, Via NO.= 16)

+2.5VSP (1A, 40mils, Via NO.= 2)

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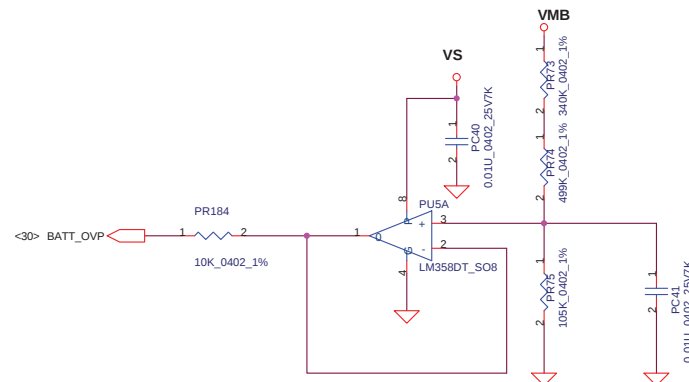
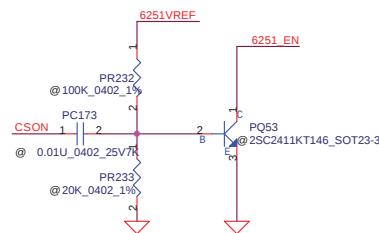
75W Iadapter=0~3.947A PR49=0.02 ohm CP=3.71A PR66=10.7K
 90W Iadapter=0~4.737A PR49=0.015 ohm CP=4.459A PR66=19.6K
 120W Iadapter=0~6.315A PR49=0.010 ohm CP=5.936A PR66=19.6K PR69=4.53K



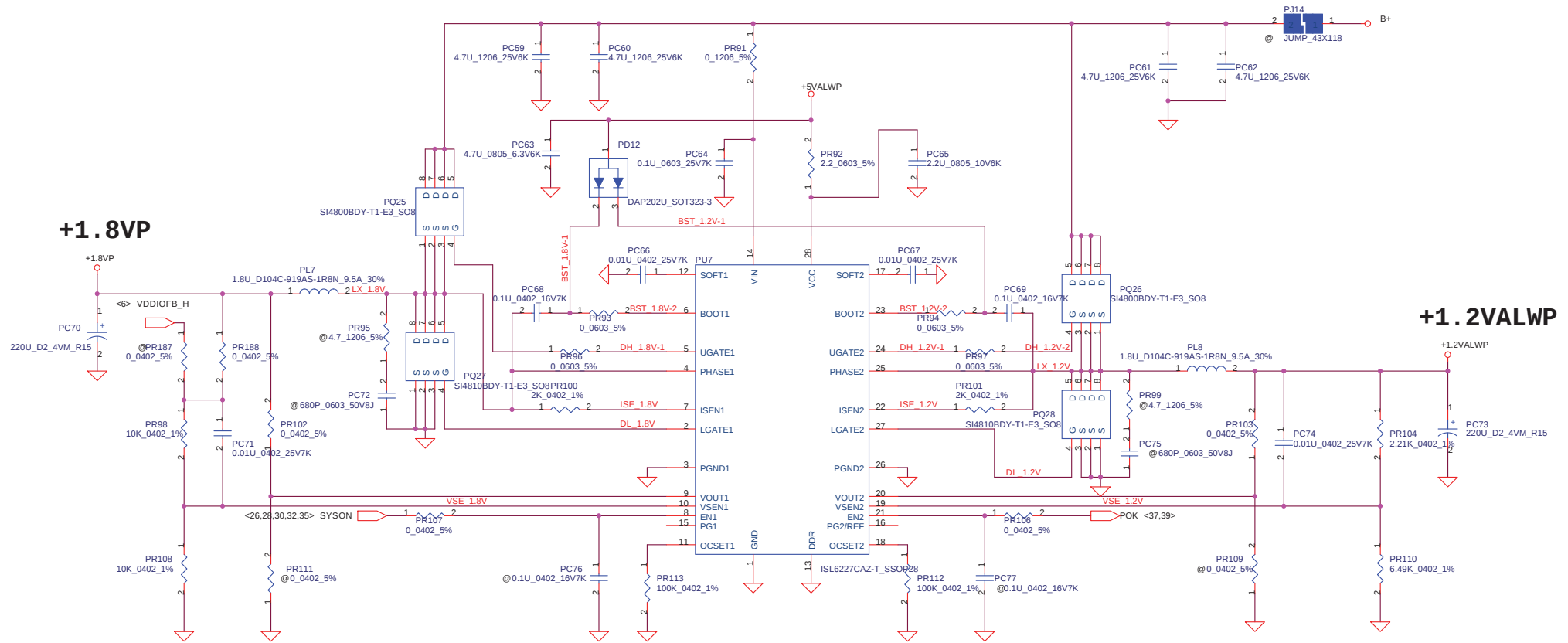
IREF=1.016*Icharge
IREF=0.508V~3.048V

CC=0.5~3A
CV=12.6V(6 CELLS LI-ION)

BATT Type	ALI/MH#	Charge Current	IREF
3 CELL	3.3V	1.5A	1.524V
6 CELL	3.3V	3.0A	3.048V
9 CELL	3.3V	3.0A	3.048V

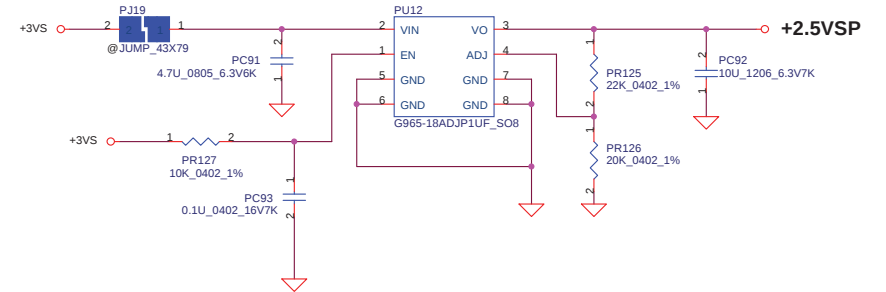
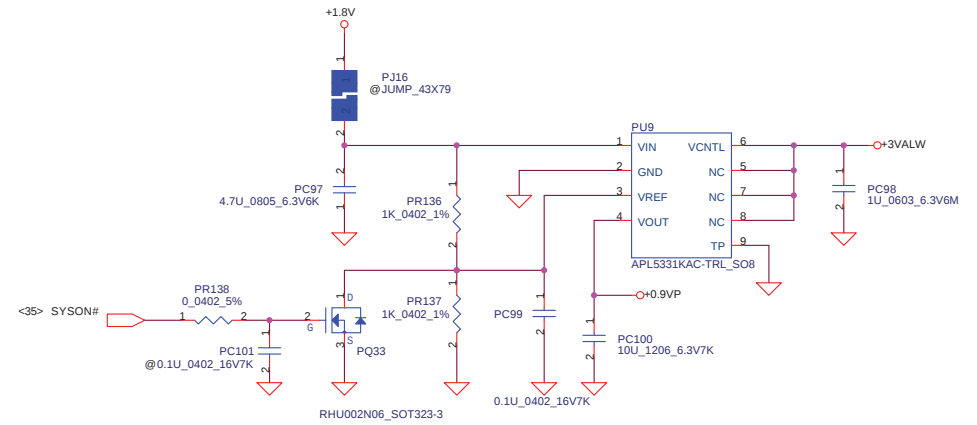
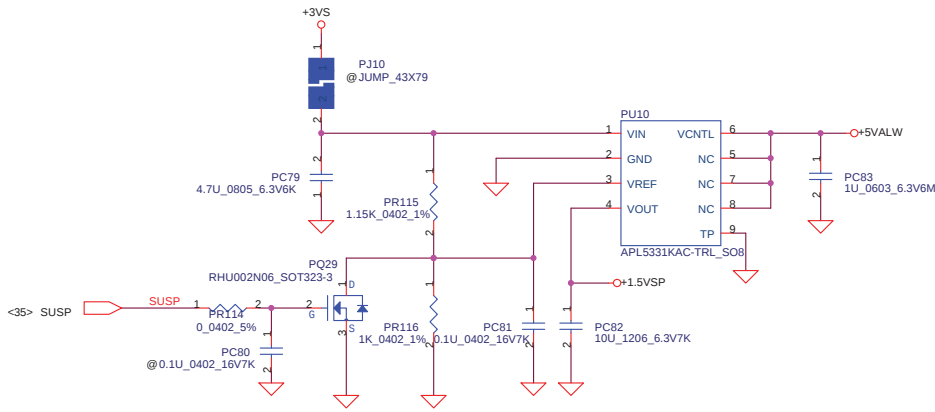


LI-3S :13.5V---BATT-OVP=1.5V
LI-4S :18V---BATT-OVP=2V
BATT-OVP=0.111*BATT+



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				1.8V / 1.2V	
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POWER PIR LIST

	page	Reason for change	Modify list
DVT	37	Design change PF2 value	Change PF2 Fuse from 12A to 15A
	38	Design change PU4 schematic	Add PR117,PR118.
			Change value PC29,PC32,PR56,PR57,PQ18
			Remove PR232,PR233,PC173,PC105
	42	improve CPU-core ripple	Change PR214,PR222 from 100 to 10
			Change PC155,PC169 from 0.22u to 0.1u
			Change PR213 from 31.6K to 20K
		Add EMI soultion	Change PC150,PC153,PC168 from 680P to 220P
			Change boost resistors PR193,PR215 from 0 to 2.2
			Change low-side mosfet PQ43,PQ44,PQ48,PQ49 at CPU-core.
PVT	37	Design change PH1 temperature set value	Change PR36 from 22K to 15.4K
Pre-MP	37	Design change PH1 temperature set value	Change PR44 from 22K to 15.4K

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HW4 Product Improvement Record (P.I.R.)

Phase: to		Date:			Writer:		
Page#	Action Plan (add; del; change)	Location or Net_List	Before value (Attached file)	After value (Attached file)	Detail Discretion and Root Cause	Rev.	DL/DM Check

01. 2007/2/12 P30

Rev 0.3 LA-3631P Implement items:

- 01. P06 Update THERMTRIP# control circuit, follow AMD request.
- 02. P07 Change C652 and C557 to SGN00000800
- 03. P08 Swap RP20 signals for DDR shielding.
- 04. P11,P13,P24 Set BOM Structure for UMA@, DVD@
- 05. ALL Change 2N7002 main source to SB770020010 for unit.
- 06. P27 Add D6, D3, ESD Diod for EMI, Chenge Encoder, SW6, PN to DEB00000600
- 07. 15 Unit Q1,Q3,Q52 w/ same part.
- 08. 24,P34 Change D31 and D28 to SC1BAS16000
- 09. P14 Add C13,C16,C21 with 22P for EMI.
- 10. P16 Change R436 and R437 to 120 Ohm to meet ADM request
- 11. P29 Remove R113, R117, R135 and R141 to leave chock for AMD platform
- 12. P28 Reserve C730~C736 by EMI request.
- 13. P21 Swap JP28 LED behaivor signals.
- 14. P28 Swap JP20 RX/TX Lanes sigals for Express Card cna't detect issue.

Rev 0.4 LA-3631P Implement items:

- 01. P24 Cut JP1.7 Pad for soldring issue.
- 02. P34 Change Q46 to SB934090000 for Fan can't meet Max. speed issue.

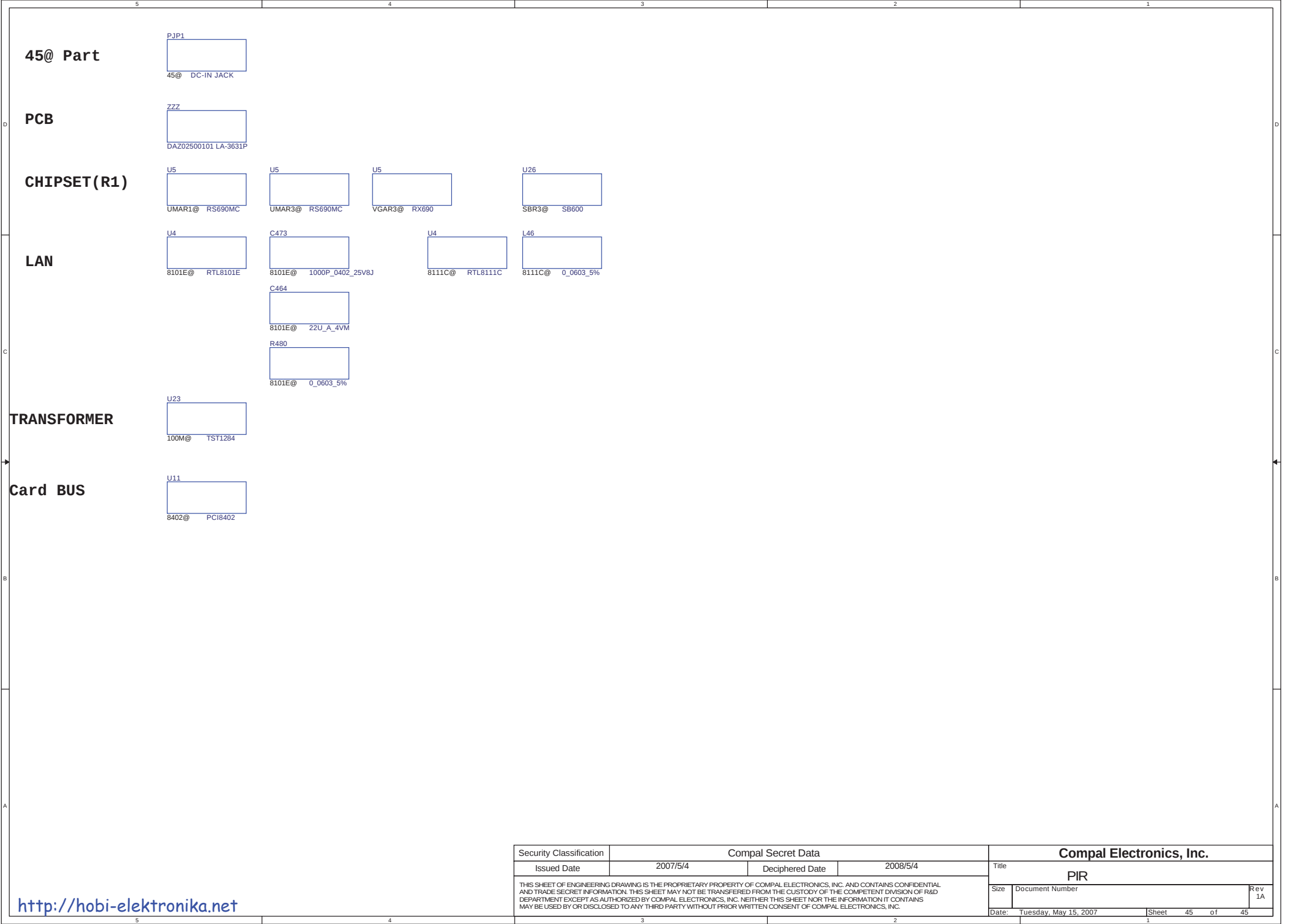
Rev 1.0 LA-3631P Implement items:

- 01. P22 Reserve C737, C738 for EMI solution
- 02. P6 Reserve R490 for PROCHOT funcation
- 03. P11 Add R488, R489 for LCD flash when boot issue

Rev 1A LA-3631P Implement items:

- 01. P22 Add R196 and C320 in BOM as EMI requirment.
- 02. P17 Add U35 and C740, reserve R1178 for LAN Leakage problem
- 03. P19 Change C647 to 22u for sequence and L59 to DCR is 0.40hm to meet AMD requirement.
- 04. P20 Change R431 and R430 to 24K; R1176 and R1177 to 19.2K, follow ATI ER.
- 05. P13 Change R369 from 330hm to 900hm Bead.
- 06. P30 ENE's recommend, change back C541 and C542 from 27P to 15P.
- 07. P06 Reserve pull up resistor R490 for H_PROCHOT#
- 08. P24/P29 Swap USB2+/- and USB8+/- for CAMERA problem.
- 09. P14/P20 Change D10 and D29 part to meet HDMI and CRT power requirment.
- 10. P20 Update HDMI Hot Plug DET circuit, to add U34, C739.

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